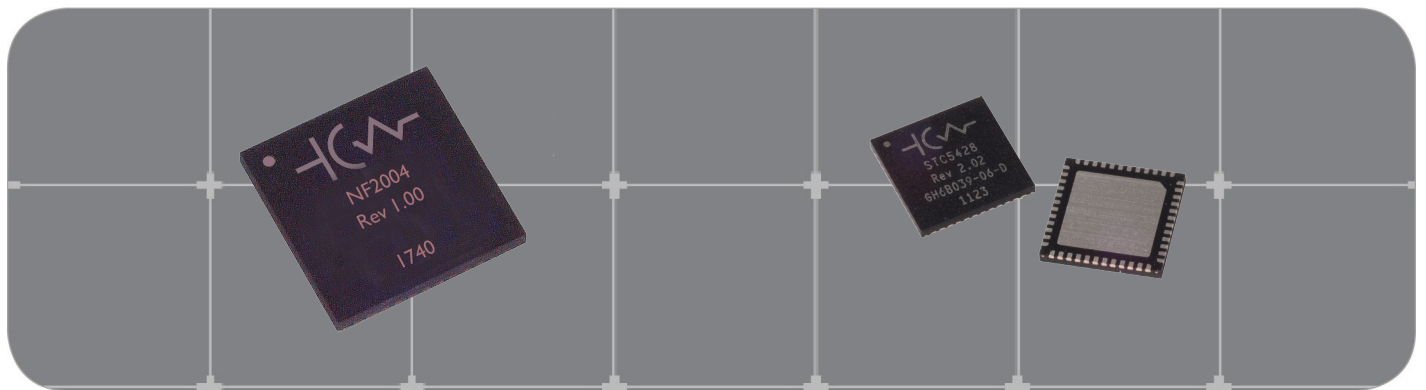


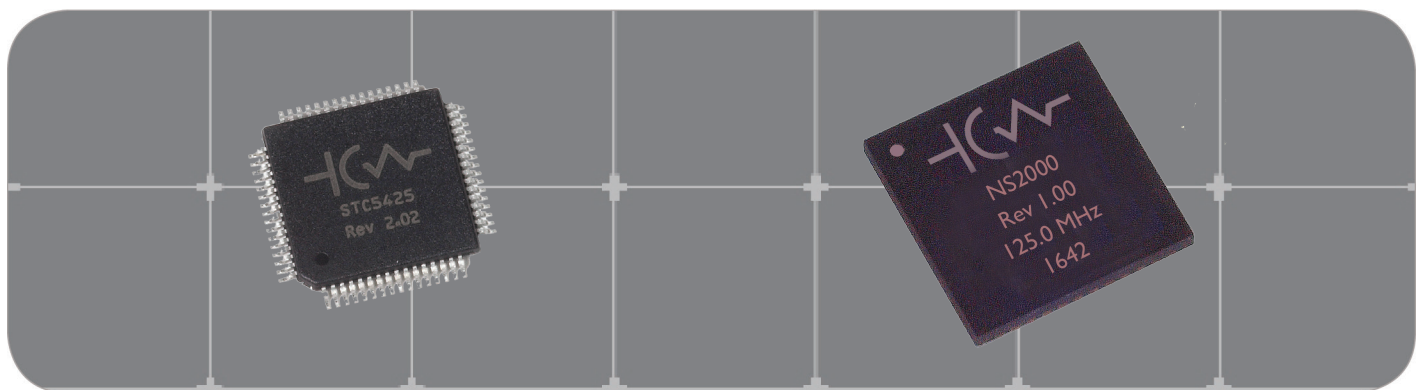
TIMING SOLUTIONS

PRODUCT GUIDE

THE CONNOR-WINFIELD CORPORATION



“System Synchronizing ICs
with Analog PLL and Low Jitter Outputs”



**CONNOR
WINFIELD**

Global Timing Solutions
for Over 50 Years



CONNOR WINFIELD



At Connor-Winfield we take exceptional pride in providing solutions to your frequency control design requirements. Our ongoing goal is to always supply you with the right solution for your product.

With this ever-prevailing philosophy, we will work with your design team to assure complete compatibility with your final product design — even if that product does not currently exist. By participating at the front end of your design cycle, we will recommend the exact product you need...or co-develop to match your exact and precise design requirements.

This Timing Product Guide is intended to as an overview of the full line of Connor-Winfield timing products. Please visit our website for a more comprehensive look at our product offering.

www.conwin.com

**Celebrating
50+ Years
of Timing
Excellence**

Integrated Timing Solutions –

“System Synchronizing IC with Analog PLL and Low Jitter Outputs”

Since 1963, Connor-Winfield (CW) has been a leader serving the OEM oscillator and crystal marketplace. Since its inception, CW has continued to develop products and evolve time and frequency technology in concert with the evolution of communication systems. Total timing system design became the natural evolution of Connor-Winfield’s experience and expertise. Incorporating proven crystal, VCXO, TCXO and OCXO and PLL technologies into system level designs, CW is able to control the fundamental requirements of communication system support. With its 50+ year history of precision frequency control and low noise signal generation, Connor Winfield is in a unique position to provide complete timing systems for network timing sync architecture, frequency regeneration and timing signal generation. Connor-Winfield’s timing architecture began with subsystems and module offerings, and now culminating in highly flexible programmable integrated circuits with second and third generation designs offering ultra-low jitter, programmable frequency outputs. Our system level focus eliminates the need for dedicated timing expertise and the need to engineer and test individual filters, clocks and control functions; dramatically reducing design time and accelerating time to market. You get a system level solution, complete and ready to perform within the precise parameters of network timing requirements and your system communications/control specifications. All Connor-Winfield network timing products are designed to meet and exceed Telcordia/ITU standards including GR-1244 and GR-253, as well as G.812, G.813, G.8262 and G.8263, G.8272 PTP and IEEE1588 specifications.

Frequency components such as clocks and crystals are used in a variety of electronic equipment, not all of which require the precision and low noise characteristics demanded by communication system applications. Connor Winfield’s timing components have been designed specifically to support the mission critical requirements of today’s most sophisticated network and communication systems. Connor Winfield, through its long history of direct customer involvement, understands the nuanced behavior and characteristics of the products it designs and manufactures as they relate to system level performance. This experience is incorporated into the products and services offered to our customers.

Reference Design

After a discussion to understand the architecture of your network element, Connor-Winfield engineers can recommend a timing solution that exactly matches your requirements. The reference design will then include an ASIC and Connor-Winfield software, along with a functional block diagram and recommendations for external components. This allows the OEM to lay the design out on their board and manage all aspects of the material supply of the components.

All Connor-Winfield network timing products meet Telcordia/ITU standards including GR-1244, GR-253, G.812, G.813, as well as G.8282 and G.8263 specifications.

SOLUTIONS

Integrated Timing Solutions – “System Synchronizing IC with Analog PLL and Low Jitter Outputs”

Connor-Winfield's Timing ICs are single chip solutions for timing solutions and line card operations in SDH, SONET, and Synchronous Ethernet applications. All ICs have freerun, holdover and reference switching capabilities.

Control monitoring is done through an SPI bus. STC54xx series conform to GR-1244-CORE, GR-253-CORE, G.812 (Type IV), G.8262 (Option 1 & 2), G.812 and G.813 (Option 1 & 2). STC3800 conforms to G.812 (Type III) and G.8263. These modules address all reference monitoring, selection, filtering, synthesis and control.

STC5420



STC5415



STC5423



STC5425



STC5428



The RoHS compliant **STC54xx Series** accepts up to 12 clock reference inputs and generates up to 10 synchronized clock outputs. Synchronized outputs may be programmed for a wide variety frequencies including Nx8kHz, OC-N, Ethernet frequencies and framing pulse clocks. Reference inputs are individually monitored for activity and quality.

The STC54xx Series are clocked by either a TCXO or OCXO 12.8MHz external oscillator. A well-chosen external oscillator, such as T502-12.8M or an OH300-012.8M from Connor Winfield, will allow you to meet all synchronization requirements

STC54xx IC Models	Package	Inputs			Outputs		Frame Clocks
		CMOS	LVPECL / LVDS	Ext_Sync 2k/8kHz	LVC MOS	LVPECL / LVDS	
STC5420	TQFP100	10	2	1	6	2	2k/8k
STC5415	TQFP100	5	2	1	1	1	2k/8k
STC5423	TQFP100	2	0	0	5	2	2k/8k
STC5425	TQFP100	5	2	3	1	1	2k/8k
STC5428	TQFP100	10	2	1	6	2	2k/8

STC54xx IC Models	Timing Generators	PLL BW (Hz)	M/S Xref	Application	Compatible Cross Reference
STC5420	T0/T4	0.1 - 103	Yes	Timing Card Redundant Master/Slave	ACS8520 IDT82V3380
STC5415	T0	13 - 103	No		-
STC5423	T0/T4	0.1 - 103	No	Timing Card	ACS8523
STC5425	T0	13 - 103	No	Protection Switching	ACS8525 ACS8525A
STC5428	T0/T4	0.1 - 103	No	Timing Card Redundant Master/Slave	

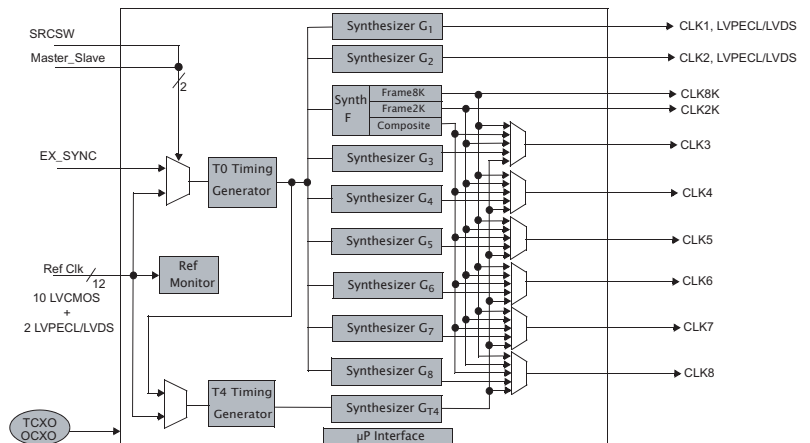


STC3800

Made for Stratum 3E, The STC3800 supports the Master or Slave mode of operation for redundant designs. In master mode, the device operates in Free Run, locked or Hold Over. In slave mode, the output clocks are locked to the master's primary Sync_Clk or 8 kHz synchronous clock output and are phase offset adjustable.

- Input reference frequency are automatically detected
- Supports hardware pins to select active reference
- Four output signals: one selectable up to 155.52 MHz, one fixed at 8 kHz, one multi frame sync fixed at 2 kHz, and 1.544 MHz or 2.048 MHz BITS output
- Hit-less reference switching
- Better than 1 ppb Holdover accuracy
- Configurable bandwidth filter for Stratum 3 or 3E
- Supports SPI

STC5420 Functional Block Diagram



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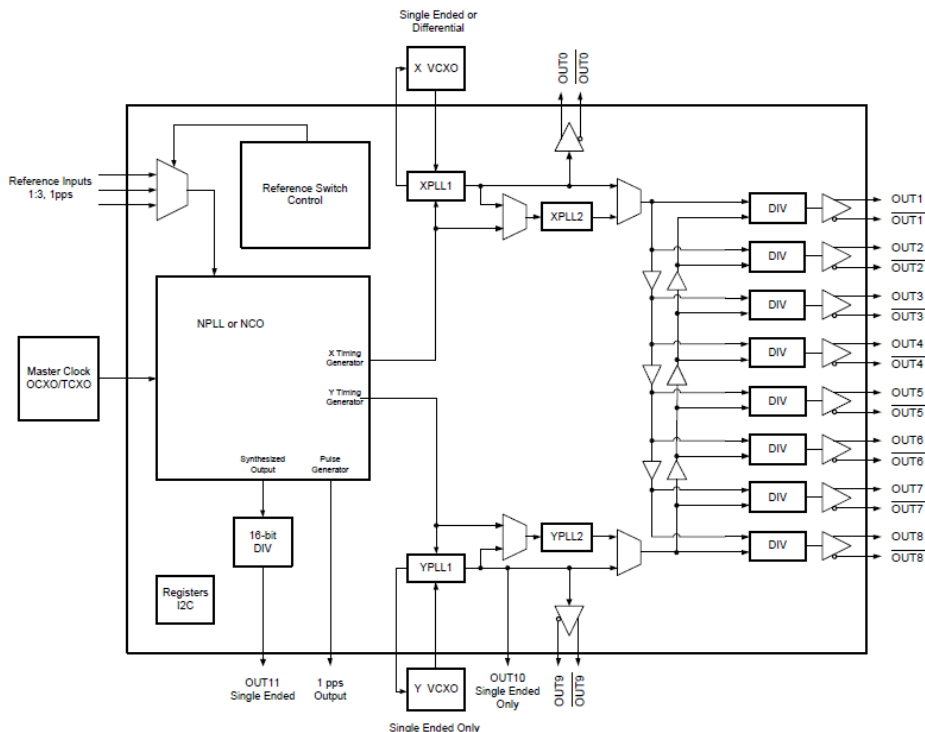
All models have free run, holdover, hitless reference switching, adjustable filter bandwidths, input reference qualification, LOL/LOS alarm indication and master/slave operation. Control and monitoring is done through I2C bus or stateful pin indicators. Main outputs derived from external VCXO(s) and very low jitter <1 ps rms jitter (12 kHz –20 MHz).

NS2000 Overview

The NS2000 and NS2004 design architecture incorporates sophisticated analog and Numerical PLL technology to provide up to 23 phase/frequency locked output(s) at frequencies from 1Hz to 800 MHz, including a 1PPS output phase aligned to the 1PPS source to less than 1ns resolution. The NS2000 supports three reference inputs including inputs from 1PPS sources and single ended clock sources at frequencies from 1 kHz to 125MHz. An external precision OCXO or TCXO provides the system clock for various holdover performance options as well as various filter bandwidth options. A variable bandwidth filter (0.25 m Hz to 50 Hz) enables the support of various network element classifications and ITU standards. Up to two external disciplined VCXOs provide the output characteristics for phase noise and jitter performance for any combination of 10 differential or 23 single ended clock outputs (8 differential and 18 single ended for NS2004) with output jitter performance options of sub 100fs RMS (12 kHz to 20MHz).

NS2000 Features

- 3 Reference inputs (1 ~ 3 can accept 1pps or LVCMOS reference signal/ clock)
- Automatic and controllable hit-less switching capability
- Programmable phase alignment of outputs to reference inputs (including 1 pps) signal
- Locked, HO, & Free-run indication. Holdover options available to .001ppb resolution
- 1Hz to 800 MHz clock output frequency range
- 10 differential or up to 23 single ended Low Jitter Clock Outputs
- Programmable output transmitters (programmable as either 1 LVPECL, 1 LVDS or 2x LVCMOS output)
- Low jitter clock outputs (less than .3ps RMS (12kHz to 20MHz) with options for sub 100fs)
- Programmable bandwidth settings for multiple applications
- I2C Interface for system communication and interrogation.
- 10 x10 mm 88 pin QFN surface mount package



NS2000 Functional Block Diagram



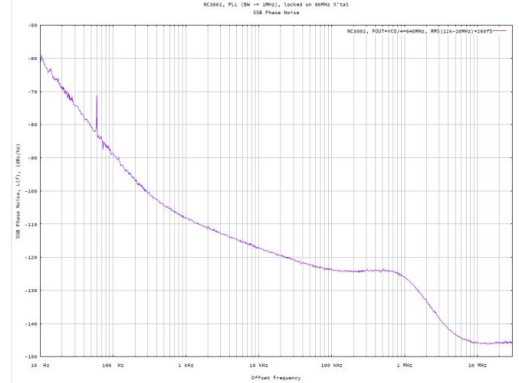
SOLUTIONS

Integrated Timing Solutions – “System Synchronizing IC with Analog PLL and Low Jitter Outputs”

All models have free run, holdover, hitless reference switching, adjustable filter bandwidths, input reference qualification, LOL/LOS alarm indication and master/slave operation. Control and monitoring is done through I2C bus or stateful pin indicators. Main outputs derived from external VCXO(s) and very low jitter <1 ps rms jitter (12 kHz -20 MHz).

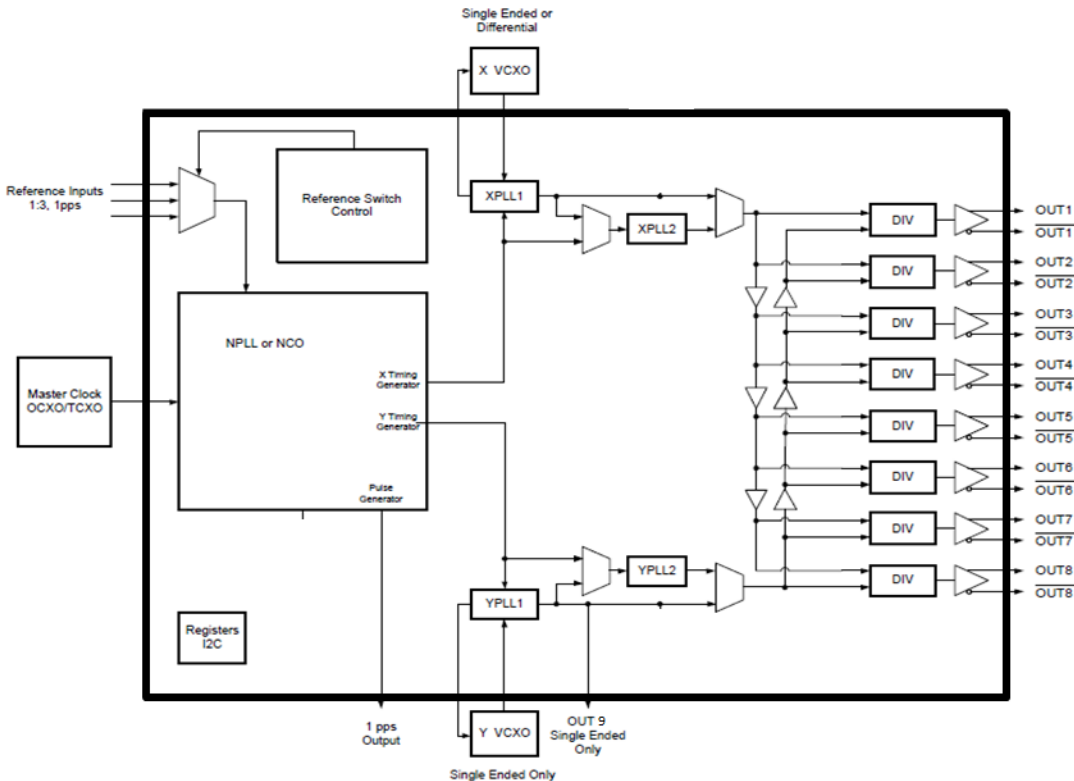
NS2004 Features

- 3 Reference inputs (1 ~ 3 can accept 1pps or LVCMOS reference signal/ clock)
- Automatic and controllable hit-less switching capability
- Programmable phase alignment of outputs to reference inputs (including 1pps) signal
- Locked, HO, & Free-run indication. Holdover options available to .001ppb resolution
- 1Hz to 800 MHz clock output frequency range
- 8 differential or up to 17 single ended Low Jitter Clock Outputs plus 1PPS output pulse generator
- Programmable output transmitters (programmable as either 1 LVPECL, 1 LVDS or 2x LVCMOS output)
- Low jitter clock outputs (less than .3ps RMS (12kHz to 20MHz) with options for sub 100fs)
- Programmable bandwidth settings for multiple applications
- I2C Interface for system communication and interrogation.
- 8 x8 mm 68 pin QFN surface mount package



640MHz LVPECL Output using 80MHz VCXO 250fs (12kHz-20MHz)

Model	Volt	Input Ref Freq.	Reference Inputs	Output Osc. Freq.	Number of Outputs	Output Type	Free Run
NS2000	3.3	8 kHz - 125 MHz	3	1Hz - 800.0 MHz	10/23	Diff/CMOS	Yes
NS2004	3.3	8 kHz - 125 MHz	3	1Hz - 800.0 MHz	8/18	Diff/CMOS	Yes



NS2004 Functional Block Diagram

Check on-line for the most up to date RoHS compliant products



T I M I N G P R O D U C T S

Integrated Timing Solutions – “System Synchronizing IC with Analog PLL and Low Jitter Outputs”

Synchronous Clock Generator IC - A

Connor-Winfield’s Synchronous Clock Generator Line Card ICs are designed to be reference clock sources which lock to one or two backplane references from the Timing/Sync Cards. Dual reference inputs are designed to switch hitlessly using select pins. Locked bandwidths range from 3 Hz to 50 Hz to achieve excellent jitter attenuation. A Loss-of-Lock alarm is available with manual or automatic Freerun operation pending external clock/crystal source applied. All SCG IC products are well suited for use supporting frequency translation and jitter attenuation in line cards, service termination cards and similar functions to provide reliable reference, phase locked synchronization for OTN, PHD, SONET, SDH and Synchronous Ethernet network equipment or as an IEEE1588 Packet Processor Servo Disciplined Device.

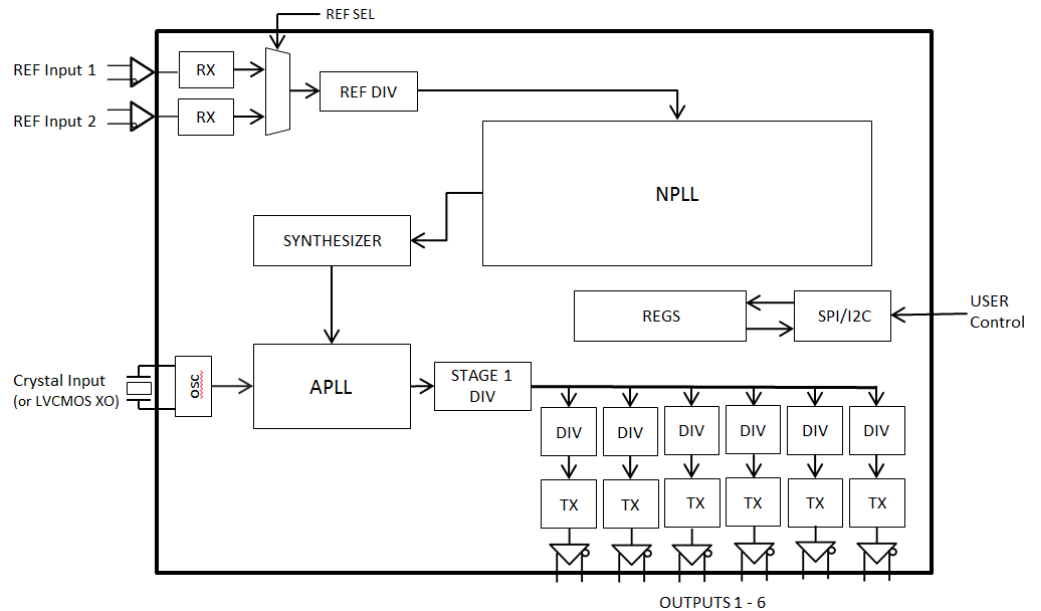
NL3106 Overview

The NL3106 design incorporates a sophisticated synthesizer in conjunction with a low noise APLL to offer “any frequency” capability with jitter performance less than .2ps from 12kHz to 20MHz. With six programmable output transmitter ports, the NL3106 can generate either six differential (programmable as either LVPECL or LVDS) or 12 LVCMOS outputs.

The NL3106 can generate frequencies in the range from 1KHz to 800MHz. In NPLL mode, its numerical PLL can accept two external reference inputs from either differential or single ended sources. In NCO mode, the NL3106 internal NCO can be accessed via its SPI serial port to support clock generation locking to external IEEE1588 servo systems via offsets from a local oscillator on one reference input port. The NL3106’s analog PLL (APLL) is supported by a single crystal to support low jitter clock generation. The NL3106 operates at 3.3V and comes packaged in a 48 pin 7x7mm QFN. (Also available in 6x6mm package with 4 output transmitter circuits (model number NL3104).

Features

- Hitless switching between reference inputs
- Programmable output transmitters (programmable as either 1 LVPECL, 1 LVDS or 2x LVCMOS output)
- 20 bit divider capability at output transmitters.
- Low jitter clock outputs less than .2ps RMS (12kHz to 20MHz)
- External control through SPI/I2C of internal NCO to discipline low jitter outputs
- External EEPROM option for loading register information
- SPI or I2C Interface for active system communication



Model	Volt	Input Ref Freq.	Reference Inputs	Output Osc. Freq.	Number of Outputs	Output Type	Free Run
NL3106	3.3	8 kHz - 800 MHz	2	1.544-800 MHz	6/12	Diff/CMOS	Yes
NL3104	3.3	8 kHz - 800 MHz	2	1.544-800 MHz	4/8	Diff/CMOS	Yes

Model	Ht. mm	Size (L x W) mm”	RoHS	REACH SVH 174
NL3106	1	7x7	6/6 Compliant	Compliant
NL3104	1	6x6	6/6 Compliant	Compliant

SOLUTIONS

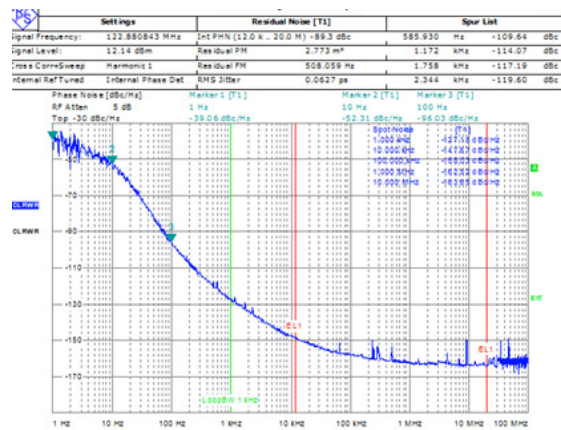
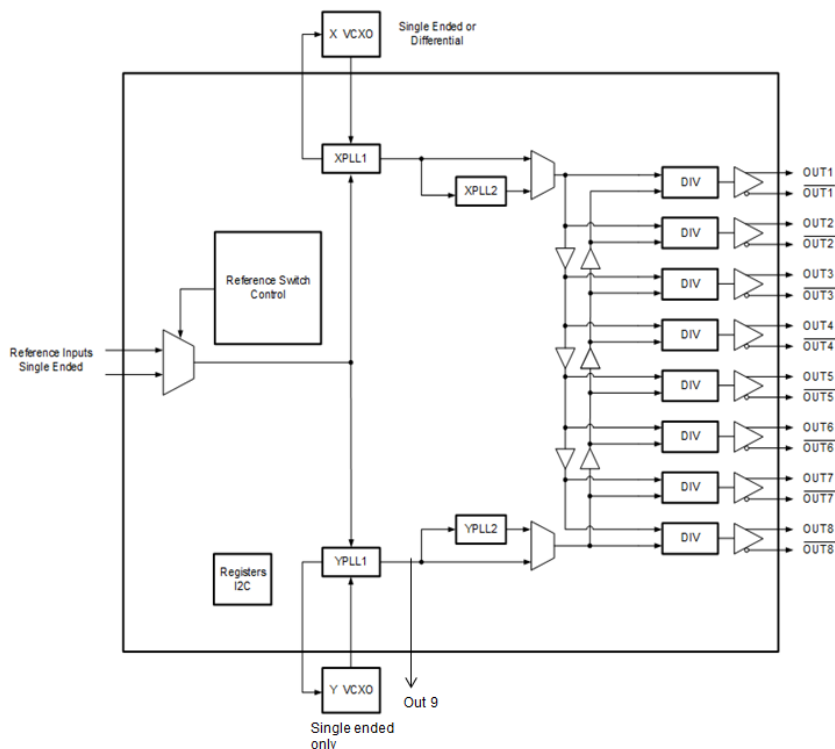
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Frequency Translators convert up to two reference input frequencies from 8 kHz to 170 MHz to one or more output frequencies up to 800 MHz (e.g. 25 MHz to 155.52 MHz and/or 19.44 MHz to 156.25 MHz). Input levels are LVCMOS Output levels can be programmed to be either LVCMOS, LVPECL., or LVDS. Outputs are very low jitter (<0.3 Ps RMS 12 kHz-20 MHz). Input frequency tracking ranges cover SONET to Ethernet requirements. Lock alarm indication is standard. Common applications for frequency translator modules include clock multiplication, clock jitter attenuation and regeneration, cross frequency domain translation and distribution of backplane/midplane distributed NE base rate clocks.

NF2004 Overview

The NF2004 design implementation is intended to be flexible offering multiple configurations that can be used to optimize low noise frequency generation and/or frequency translation. The design architecture incorporates sophisticated analog PLL scheme which can provide up to 17 phase/frequency locked single ended output(s) or 8 differential (LVPECL or LVDS) outputs at frequencies from 1 kHz to 800 MHz. The NF2004 supports two reference inputs from single ended clock sources at frequencies from 8 kHz to 125MHz. Up to two external disciplined VCXOs provide the output characteristics for phase noise and jitter performance.

The VCXO signals can be either passed through directly to eight programmable output transmitters, maintaining their low phase noise characteristics or they can support a second order high frequency PLL for clock synthesis via the NF2004’s 20 bit divider capability at each output transmitter port. Output jitter performance, depending upon the configuration chosen, can achieve levels of 70fs RMS (12 kHz to 20MHz) for direct signal pass through or sub .3ps for synthesized clock outputs.



Phase noise generated from YPLL1:
122.88MHz 63fs (12kHz-20MHz) (using Connor Winfield model V773T-122.88MHz LVCMOS 5x3.2mm VCXO)

Parameter	Specification
Voltage	3.3V +/- 5%
Power	based on configuration (100ma with outputs tri-stated) Outputs add: LVPECL 50ma, LVDS 20Ma, LVCMOS 8 ma
Temperature	-40 to 85 c Industrial temp range operation
Reference Frequency	Single ended clock input 8KHz – 125MHz
Low Jitter Clock Output Frequency	1Hz to 800 MHz
Dimensions	8 x 8 x 1mm 68 pin QFN package

Integrated Timing Solutions – “System Synchronizing IC with Analog PLL and Low Jitter Outputs”

Multi-Output Clock Generator ICs -

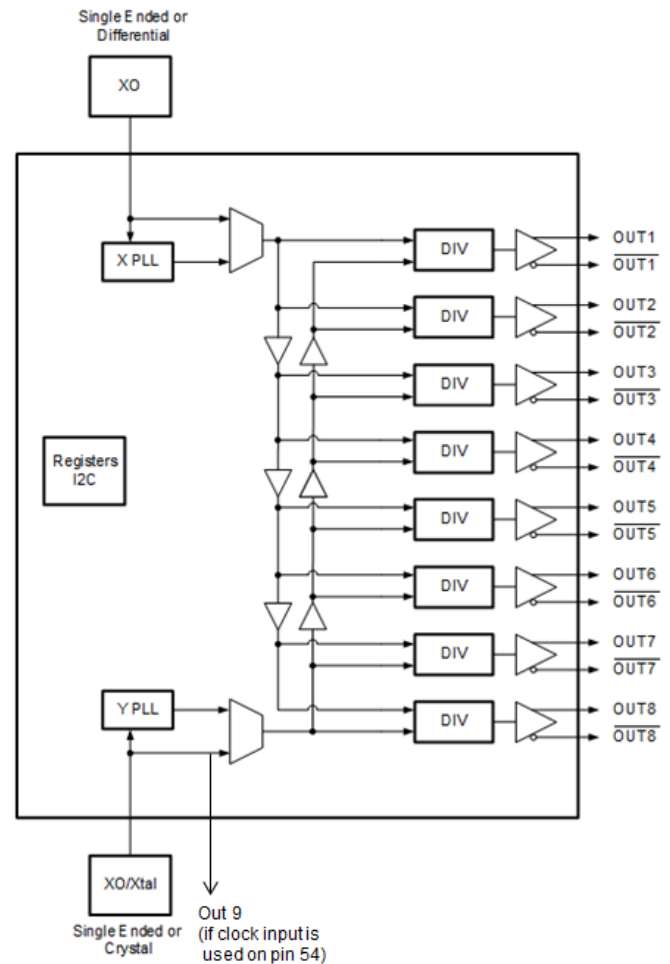
Connor-Winfield’s Multi output clock generators are designed to be low noise clock sources where distribution of multiple clock signals are required to support a variety of on board ICs and clock rates.

NC2004 Overview

The NC2004 is a highly integrated multi output clock generator and signal translation device. This design implementation is extremely flexible in providing low noise frequency generation and/or signal level translation capability. The design architecture incorporates Connor-Winfield’s second generation analog PLL technology to provide up to 17 output(s) at frequencies ranging from 1Hz to 800 MHz, depending upon the input reference option chosen. One or two external signal sources determine the output characteristics for phase noise and jitter performance for any combination of 8 differential or 17 single ended clock outputs with output jitter performance options of sub 100fs RMS (12 kHz to 20MHz). Configurations can be controlled using I2C interface, external EE PROM or can be preconfigured in nonvolatile memory (OTP) at the factory. One or two external signal sources can be accepted from a crystal unit, a single ended LVCMOS signal, a differential (LVDS or LVPECL) signal or a combination of those. When using a crystal unit, 100fs jitter performance is achievable.

Features

- 1Hz to 800 MHz clock output frequency range
- 8 differential or up to 17 single ended Low Jitter Clock Outputs
- Programmable output transmitters (programmable as either 1 LVPECL, 1 LVDS or 2x LVCMOS output)
- 20 bit divider capability at output transmitters 1-8.
- Low jitter clock outputs of less than .25ps RMS (12kHz to 20MHz) with options for sub 100fs.
- Signal translation from LVCMOS to LVPECL/LVDS or Vice versa
- External EEPROM for loading or I2C Interface for system communication
- 3.3V supply
- 8x8 mm 68 pin QFN surface mount package

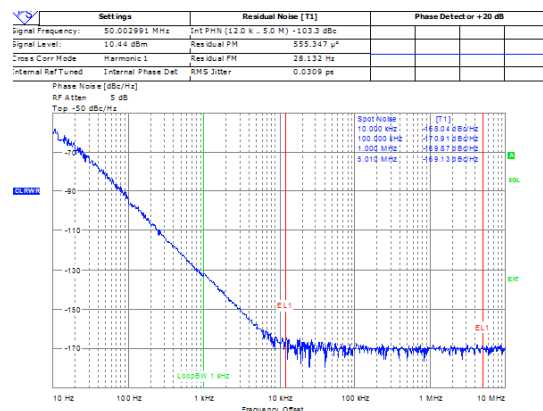


Support Clock Oscillator for NC2004 and NC3106/04

The Connor-Winfield XK372 3.2x2.5 mm, LCMOS, Surface Mount, Crystal Controlled Oscillators (XO) are designed for applications requiring low jitter and tight frequency stability.

Features:

- Supply Voltage: 3.3V Operation
- Frequency Tolerance: ±25 ppm, ±50 ppm, ±100 ppm
- Temperature Range: -40 to 85°C
- LVCMOS Output Logic
- Tri-State Enable/Disable Pad 1
- Low Jitter < 0.1ps RMS (-170dB noise floor)
- 3.2x2.5 mm Ceramic Surface Mount Package



Integrated Timing Solutions – “System Synchronizing IC with Analog PLL and Low Jitter Outputs”

Multi-Output Clock Generator ICs -

Connor-Winfield’s Multi output clock generators are designed to be low noise clock sources where distribution of multiple clock signals are required to support a variety of on board ICs and clock rates.

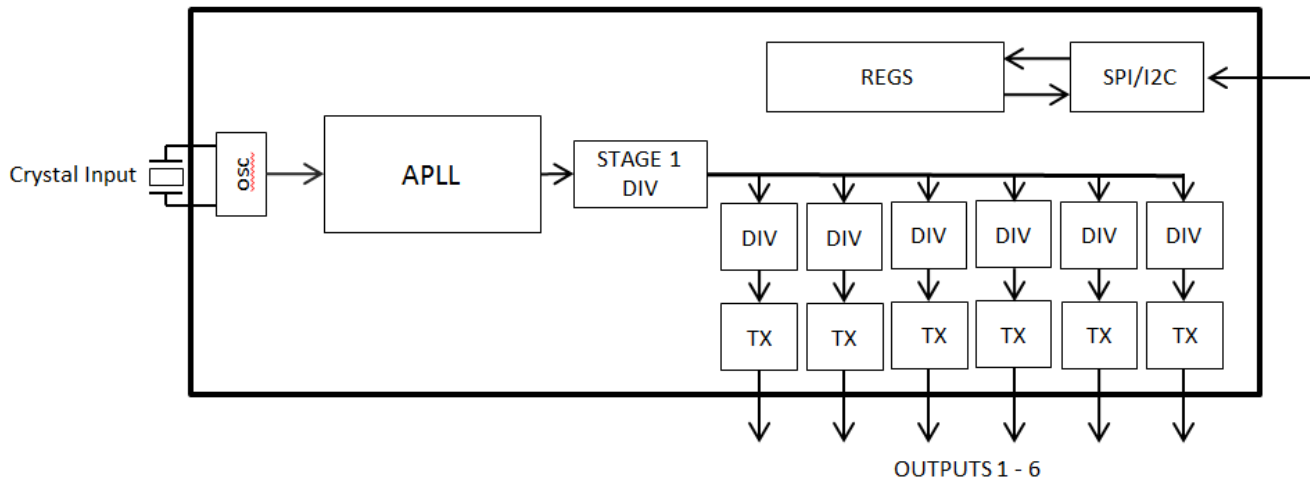
NC3106/04 Overview

The NC3106 and NC3104 IC family offers a simple but flexible design architecture providing multi output, low jitter clock generation. This third generation design incorporates a sophisticated synthesizer in conjunction with a low noise APLL to offer “any frequency” capability with jitter performance less than .2ps from 12kHz to 20MHz. With six programmable output transmitter ports, the NC3106 (four on the NC3104) can generate either six differential (programmable as either LVPECL or LVDS) or 12 LVCMOS outputs.

Incorporating a two stage divider scheme, the NC3106/04 can generate frequencies into the range of 1KHz to 800MHz. The NC3106’s analog PLL (APLL) is supported by a single crystal to support low jitter clock generation. The NC3106 operates at 3.3V and comes packaged in a 48 pin 7x7mm QFN. The NC3104 is packaged in a 40 pin 6x6mm QFN.

Features

- 1KHz to 800 MHz clock “any frequency” outputs
- 6 differential or up to 12 single ended Low Jitter Clock Outputs
- Programmable output transmitters (programmable as either 1 LVPECL, 1 LVDS or 2x LVCMOS output)
- 20 bit divider capability at output transmitters.
- Low jitter clock outputs less than .2ps RMS (12kHz to 20MHz)
- Factory Programming available
- External EEPROM option for loading register information
- SPI or I2C Interface for active system communication
- 7x7 mm 48 pin QFN surface mount package
- Programmable phase alignment of outputs to reference inputs



Model	Volt	Input Ref Freq.	Reference Inputs	Output Osc. Freq.	Number of Outputs	Output Type	Free Run
NC2004	3.3	1MHz-800MHz	clock/crystal	1.5KHz – 800 MHz	8/17	Diff/CMOS	Integer
NC3106	3.3	40-100MHz	clock/crystal	1.5KHz – 800 MHz	6/12	Diff/CMOS	Fractional
NC3104	3.3	40z-100MHz	clock/crystal	1.5KHz – 800 MHz	4/8	Diff/CMOS	Fractional

Model	Ht. mm	Size (L x W) mm”	RoHS	REACH SVH 174
NC2004	1	8x8	6/6 Compliant	Compliant
NC3106	1	7x7	6/6 Compliant	Compliant
NC3104	1	6x6	6/6 Compliant	Compliant

OCXO/TCXO Master Clock Options (for use with NS2000, NS2004, NF2004, NL3106)



Precision OCXOs and TCXOs for Time and Frequency Sync Standards

IEEE-1588 TOP Precision Timing - Precision timing is more critical for the development of communication networks based on IEEE-1588 timing over packet (TOP) and 100/ 400 Gigabit Ethernet synchronization technologies. Connor Winfield developed its line of OCXOs and TCXOs to specifically support the emerging IEEE 1588 V2 standards as outlined by ITU-G.8262 Option 1 and Option 2 and ITU-G.8263, ITU-G.8272 and ITU-G.8273 as well as the traditional Sonet, SDN and OTN standards G.813 and GR-1244 Stratum 3 and Stratum 3E. Many frequency options are available from stock to support a variety of network synchronization designs. Follow the links below for stock availability.

Oscillator Class	A1	A2	C2	D	E
Superset Grouping			Stratum 3, SMC & Option 2 (PDH, SONET, Sync E)	Option 1 (SDH, Sync E)	Line Card
Telecordia Clock	N/A Type 1	Stratum 3E Type III	Stratum 3 for SONET G.813 Option 2 G.8262 Option 2	N/A G.813 Option 1 G.8262 Option 1	Stratum 4
PLL Implied Bandwidth	3mHz	1mHz	0.1Hz	1Hz	14Hz
Free-run Accuracy (ppm)	N/A	±4.6	±4.6	±4.6	±32
Frequency Stability (pk-pk) at Variable Temperature (ppb)	2	10	280	2000	N/A
Frequency Stability at Constant Temperature (ppb)	±0.2	±1	±40	±10	N/A
Frequencies Available	10 MHz	10.0; 12.8; 20.0; 24.576 MHz	10.0; 12.8; 19.2; 20.0; 24.576; 40.0 MHz	10.0; 12.8; 19.2; 20.0 24.576; 40.0; 50.0 MHz	Various
Connor-Winfield Products Data Sheet Links	OX200SC-10M	OH100-600503CF OH300-600503CF	M602 T6-2	M622 T622 DOC102F	CWX Series

Master Clock Models Supporting CW Timing ICs

OCXO Model #	Thermal Stability	ADEV	Temp Range	Footprint
OH100-10M,20M, 24.576M	10ppb pk-pk, 5ppb available	1.x10-11	Commercial/IT	25x25mm
OH300-10M,20M, 24.576M	10ppb pk-pk, 5ppb available	1.x10-11	Commercial/IT	25x36mm
OH300-10M,20M, 24.576M	10ppb pk-pk, 5ppb available	1.x10-11	Commercial/IT	22x25mm
OX200SC 10M	3ppb pk-pk	1.x10-11	Commercial	25x36mm
OH4-24.576M, 20M, 19.2M	20ppb pk-pk	3x10-11	Commercial/IT	14x20mm
DOCSC-24.576M/20M/19.2M	20ppb pk-pk	3x10-11	Commercial/IT	9x14mm
TCXO Model #	Thermal Stability	ADEV	Temp Range	Footprint
T100	+/- 100 ppb	1x10-10	Commercial	5x7mm
T200	+/- 200 ppb	1x10-10	Industrial	5x7mm
TL602	+/- 140 ppb	1x10-10	Industrial	5x7mm
T602	+/- 280 ppb	1x10-10	Industrial	5x7mm
T622	+/- 1ppm	1x10-10	Industrial	5x7mm
DOT	+/- 50ppb	1x10-10	Commercial	9x14mm

CLOCK and Crystal Models Supporting CW Timing ICs

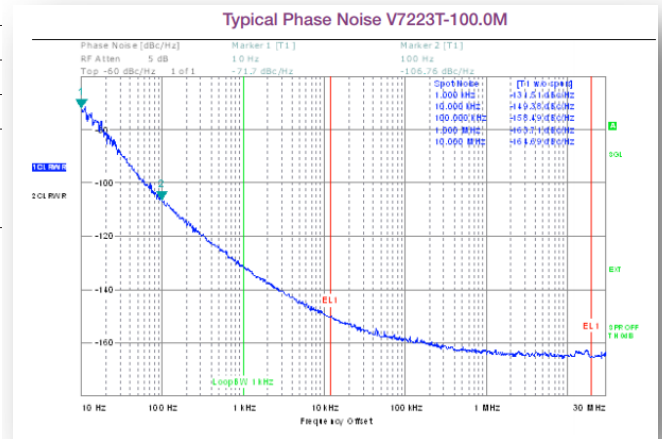
Clock Model Series	Frequency Range	Output Logic	Supply Voltage	Footprint
XF Series	1-50M	LVC MOS	1.8V	2016
XE Series	1-50M	LVC MOS	3.3V	2520
XK Series	1-50M	LVC MOS	3.3Vdc	3225
XC Series	1-50M	LVC MOS	3.3Vdc	5032
X series	10M- 160M	LVC MOS	3.3Vdc	7050
FPC series	1M-2GHz	LVPECL/LVDS/CMOS	Programmable (factory)	7050
XPC series	1M- 2GHZ	LVPECL/LVDS/CMOS	Programmable On board I2C	7050
Xtal Model Series	Frequency Range	Accuracy	Mode	Footprint
CS-035HF	>80MHz-180MHz	20ppm	Fundamental AT	5032
CS-035LF	10M-80M	20ppm	Fundamental AT	5032
CS-033HF	>100MHz-180MHz	20 ppm	Fundamental AT	3225
CS-033TX	40M-100M	20 ppm	Fundamental AT	3225
CS-032TX	40M-100M	20 ppm	Fundamental AT	2520
CS-031TX	30-80M	50ppm	Fundamental AT	2016

Support Oscillators for Connor-Winfield's Line of Timing ICs

V7223T VCXO Series

The Connor-Winfield V7223T Series models are 3.3V LVCMOS SMT 5.0x3.2mm voltage controlled crystal oscillators (VCXOs) with ultra-low jitter. With LVCMOS outputs, the V7223T series is designed for PLL applications requiring high performance and low noise. These are particularly good for straight pass through applications and dividing directly from the VCXO frequency in the NS2000, NS2004 and NF2004. (also available in 3.2x2.5mm footprint).

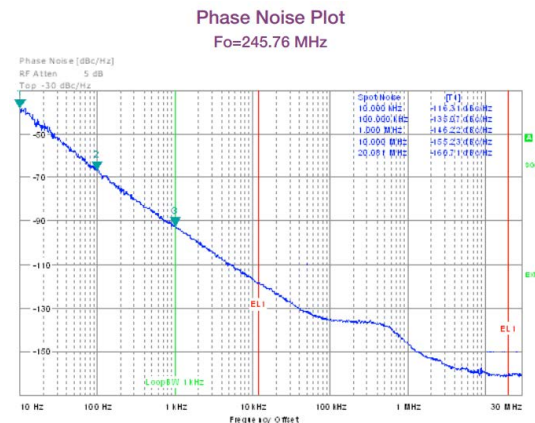
Operating	Specifications
Center Frequency (Fo)	50MHz – 156.25 MHz
Operating Temperature Range	-40 - 85 °C
Supply Voltage (Vdd)	3.3 Vdc
Supply Current (Idd)	15 mA
Absolute Pull Range:	±50ppm
Integrated Phase Jitter (BW=12kHz to 20MHz)	
Fo=100MHz	60 fs RMS
Fo=125MHz	60 fs RMS
Typical Phase Noise for 100MHz	
SSB Phase Noise at 10Hz offset	70 dBc/Hz
SSB Phase Noise at 100Hz offset	105 dBc/Hz
SSB Phase Noise at 1kHz offset	130 dBc/Hz
SSB Phase Noise at 10kHz offset	148 dBc/Hz
SSB Phase Noise at 100kHz offset	158 dBc/Hz
SSB Phase Noise at 1MHz offset	163 dBc/Hz
SSB Phase Noise at 10MHz offset	164 dBc/Hz



VL734T Programmable "Any Frequency" VCXO

The Connor-Winfield VL734T Series models are programmable 3.3V LVCMOS SMT 5x7mm voltage controlled crystal oscillators (VCXOs) using low noise PLL technology to produce ultra-low jitter clock outputs. With LVPECL or LVDS outputs, the VL734T series offers a frequency range from 10MHz to 2 GHz with sub 150fs jitter performance. These are particularly good for straight pass through applications and dividing directly from the VCXO frequency in the NS2000, NS2004 and NF2004.

Operating	Specifications
Center Frequency (Fo)	10MHz – 2 GHz
Operating Temperature Range	-40 - 85 °C
Supply Voltage (Vdd)	3.3 Vdc
Supply Current (Idd)	- - 85 mA
Absolute Pull Range:	+/- 100ppm
Integrated Phase Jitter (BW=12kHz to 20MHz)	
Fo=800MHz	140 fs RMS
Fo=245.76MHz	150 fs RMS
Typical Phase Noise for 100MHz	
SSB Phase Noise at 1kHz offset	- - 137 - dBc/Hz
SSB Phase Noise at 10kHz offset	- - 158 - dBc/Hz
SSB Phase Noise at 100kHz offset	- 160 - dBc/Hz



VCXO Models Supporting CW Timing ICs



VCXO Model Series	Frequency Range	Output Logic	Footprint	Jitter Level
V9223	2-50MHz	LVCMOS	3225	200 fs
V7223	2M-50Mhz	LVCMOS	5032	200 fs
VKB series	2M-80M	LVCMOS	7050	200 fs
V7223T	50M to 156.25M	LVCMOS	5032	60-80 fs
VB762	100-250M	LVPECL	7050	85 fs
V788	150-750M	LVPECL	7050	85 fs
PFC223	10M-2 GHZ	Programmable	7050	150-200fs
V*C223	10M-2 GHZ	LVCMOS, LVPECL, LVDS		150-200fs
VPLD	400-700MHz	LVPECL	9x14mm	50-60 fs
VBLD	80-204.8M	LVCMOS	9x14mm	50-60 fs

TIMING SOLUTIONS

PRODUCT GUIDE

THE CONNOR-WINFIELD CORPORATION

For specific product data,
performance specifications,
dimensions and ordering
information, please refer
to our website at

www.conwin.com

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ISO 9001:2008 Certification

Connor-Winfield has been ISO 9001 certified since 1995, and is currently certified under ISO's newest ISO 9001:2000 standard which ensures superior quality and repeatability in the manufacturing process.



We believe that quality begins well before our product is ever assembled.

By maintaining our ISO 9001:2000 Quality System certification, continuous improvement to our processes is a commitment we make to constantly go beyond the expectations of our customers. For us, quality is not just a technique or system. It is an all encompassing and uncompromising philosophy to produce products that not only precisely meet our customers' quality requirements, but also surpass them in every way.



Headquarters at 2111 Comprehensive Dr, Aurora, IL



Manufacturing Facility at 2359 Diehl Rd, Aurora, IL

Our Partnership Philosophy

Connor-Winfield talks about partnerships, but how do we follow through?

From design to delivery, we are committed to providing the right product when you need it to get your product to market. But the process is circular. We also track emerging developments in our customers' markets to ensure that we have the tools and data required to support your next product development effort