

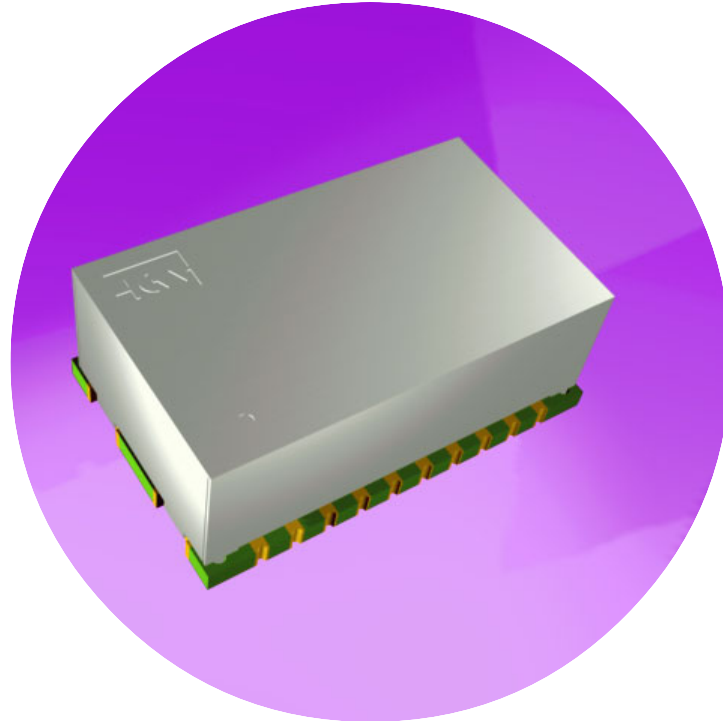
# SCG3041 Series Synchronous Clock Generators

**CONNOR  
WINFIELD**



**PLL**

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## Application

The SCG3041 is designed for use as a reference input for OC-48 Framers and SERDES. It generates less than 1 psRMS jitter over the OC-48 bandwidth.

SCG3041 is well suited for use in line cards, service termination cards and similar functions to provide reliable reference, phase locked, synchronization for TDM, PDH, SONET, and SDH network equipment. The SCG3041 provides a jitter filtered, wander following output signal synchronized to a superior Stratum or peer input reference signal.

The SCG3041 differs from SCG3040 by providing a CMOS output at 77.76 MHz.

## Features

- 3.3V High Precision PLL
- Two Differential LVPECL Outputs @ 155.52 MHz
- 19.44 MHz CMOS Input Reference
- Reference Duty Cycle Tolerant
- Low Temperature Reflow Surface Mounting
- CMOS Output @ 77.76MHz

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Revision	<b>P01</b>
Date	<b>4 NOV 02</b>
Issued By	<b>MBatts</b>

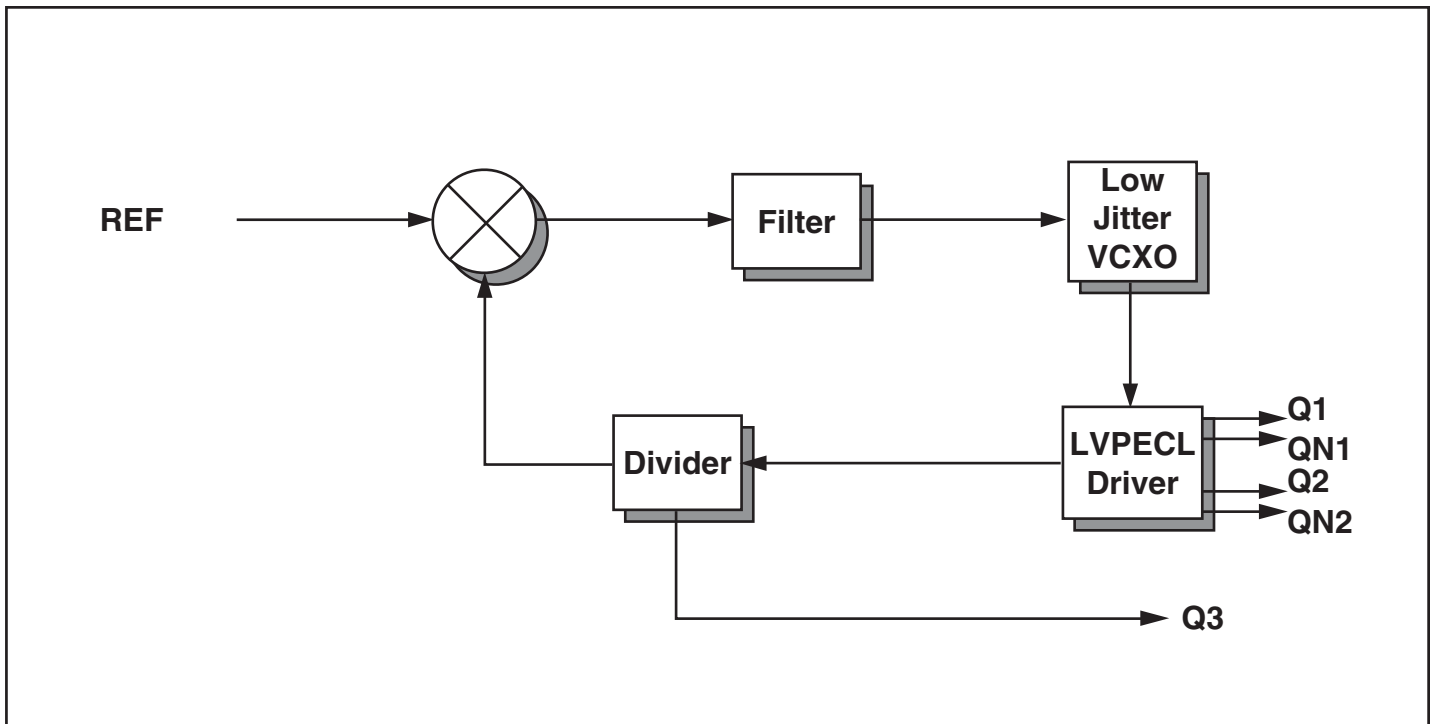
## General Description

The SCG3041 is a mixed signal phase locked loop generating 155.52 MHz LVPECL outputs from an intrinsically low jitter voltage controlled crystal oscillator. The SCG3041 is phase locked to an external 19.44 MHz reference input. The SCG3041 is ideal for applications using multiplication to obtain higher SONET frequencies.

The package dimensions are 0.75" x 1.25" x .45" on a 6 layer, designed impedance, FR4 board with castellated pins. Parts are assembled using high temperature solder to withstand surface mount reflow processes. See Fig. 4 for the solder profile.

## Functional Block Diagram

Figure 1



## Absolute Maximum Rating

Table 1

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
$V_{CC}$	Power Supply Voltage	-0.5		4	Volts	1
$V_I$	Input Voltage	-0.5		5.5	Volts	1
$T_s$	Storage Temperature	-65		150	deg. C	1

## Recommended Operating Specifications

Table 2

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
V <sub>CC</sub>	Power Supply Voltage	3.135	3.3	3.465	Volts	2, 10
I <sub>CC</sub>	Power Supply Current	-	-	270	mA	5, 6
T <sub>OP</sub>	Temperature Range	0	-	70	deg. C	
F <sub>O</sub>	Output Frequency					
	Q1,Q2	-	155.52	-	MHz	
	Q3	-	77.76	-	MHz	
F <sub>REF</sub>	Reference Frequency	-	19.44	-	MHz	
F <sub>CAP</sub>	Capture/Pull-in Range	-25	-	25	ppm	
F <sub>BW</sub>	Jitter Filter Bandwidth	-	8	15	Hz	3
T <sub>JTOL</sub>	Input Jitter Tolerance <i>(Input Jitter Frequencies ≥ 10 Hz)</i>	-	-	31.25	us	
T <sub>AQ</sub>	Acquisition Time	-	100	-	ms	4
J <sub>GEN</sub>	Jitter Generation					
	Q1,Q2	-	-	1	ps RMS	7
	Q3	-	2.5	4	ps RMS	8

## Input And Output Characteristics

Table 3

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
<b>CMOS Input Characteristics</b>						
V <sub>IH</sub>	High Level Input Voltage	2	-	5.5	V	
V <sub>IL</sub>	Low Level Input Voltage	0	-	0.8	V	
T <sub>IR</sub>	Input Reference Pulse Width	12.5	-	-	nS	
T <sub>IRF</sub>	Input Rise and Fall Time (20% to 80%)	-	-	5	nS	9
<b>CMOS Output Characteristics</b>						
V <sub>OH</sub>	High Level Output Voltage I <sub>oh</sub> = -4mA	2.4	-	-	V	V <sub>CC</sub> Min.
V <sub>OL</sub>	Low Level Output Voltage I <sub>ol</sub> = 8mA	-	-	0.4	V	V <sub>CC</sub> Max.
T <sub>RF</sub>	Output Rise and Fall Time (20% to 80%)	-	-	1	ns	5
DC	Duty Cycle	45	50	55	%	5
<b>LVPECL Output Characteristics</b>						
V <sub>OH</sub>	High Level Output Voltage	2.27	2.34	2.52	V	5
V <sub>OL</sub>	Low Level Output Voltage	1.49	1.51	1.68	V	5
C <sub>L</sub>	Output Capacitance	-	-	10	pF	
T <sub>SKREW</sub>	Differential Output Skew	-	50	-	ps	5
T <sub>RF</sub>	Output Rise and Fall Time (20% to 80%)	-	-	1	ns	5
DC	Duty Cycle	45	50	55	%	5

NOTES: 1: Operation of the device at these or any other condition beyond those listed under Recommended Operating Specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

2: Requires external regulation and supply decoupling. (22uF, 330 pF)

3: 3dB loop response.

4: From a 20 ppm step in reference frequency.

5: With LVPECL termination as defined by figure 8 (Z<sub>O</sub> = 50 Ω).

6: Maximum I<sub>CC</sub> tested at V<sub>CC</sub> = 3.46V

7: Jitter based on SONET OC-48 bandwidth ( 12 kHz - 20 MHz).

8: Jitter based on SONET OC-12 bandwidth ( 12 kHz - 5 MHz).

9: Avoid meta-stable input signals

10: V<sub>CC</sub> ramp rate must be monotonic rising. Ramp must be greater than 300 V/s from 2V to 3V.



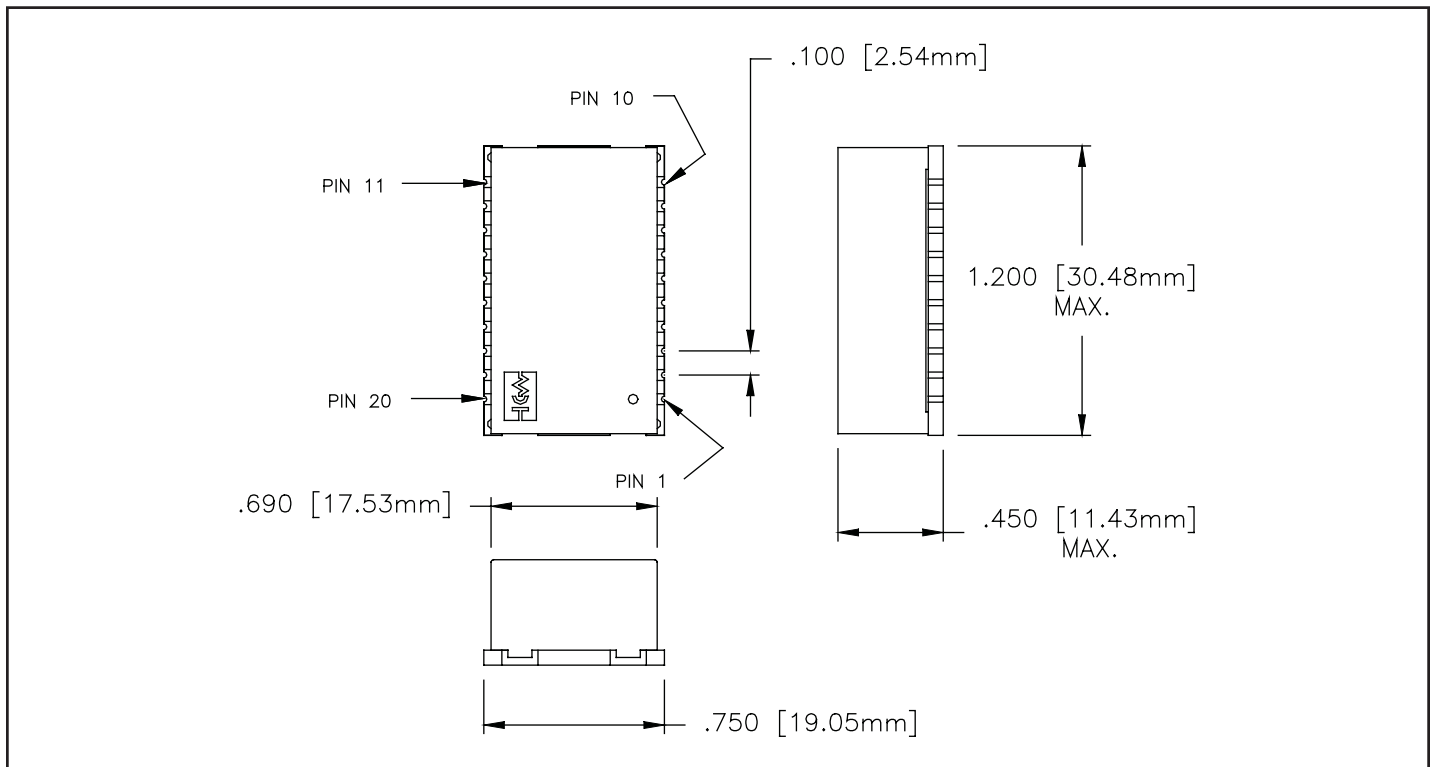
## Pin Description

Table 4

Pin #	Connection	Description
1	N/C	Do Not Connect or Route Through
2	REF	CMOS Input Reference
3	TDO	JTAG pin that is used only by Connor-Winfield for programming. Do not connect
4	GND	Ground
5	QN1	Negative LVPECL Differential Output
6	Q1	Positive LVPECL Differential Output
7	V <sub>cc</sub>	Supply Voltage Relative to Ground
8	GND	Ground
9	N/C	Do Not Connect or Route Through
10	N/C	Do Not Connect or Route Through
11	Q2	Positive LVPECL Differential Output
12	QN2	Negative LVPECL Differential Output
13	GND	Ground
14	GND	Ground
15	V <sub>cc</sub>	Supply Voltage Relative to Ground
16	TDI	JTAG pin that is used only by Connor-Winfield for programming. Do not connect
17	TCK	JTAG pin that is used only by Connor-Winfield for programming. Do not connect
18	TMS	JTAG pin that is used only by Connor-Winfield for programming. Do not connect
19	GND	Ground
20	Q3	CMOS Output

## Package Dimensions

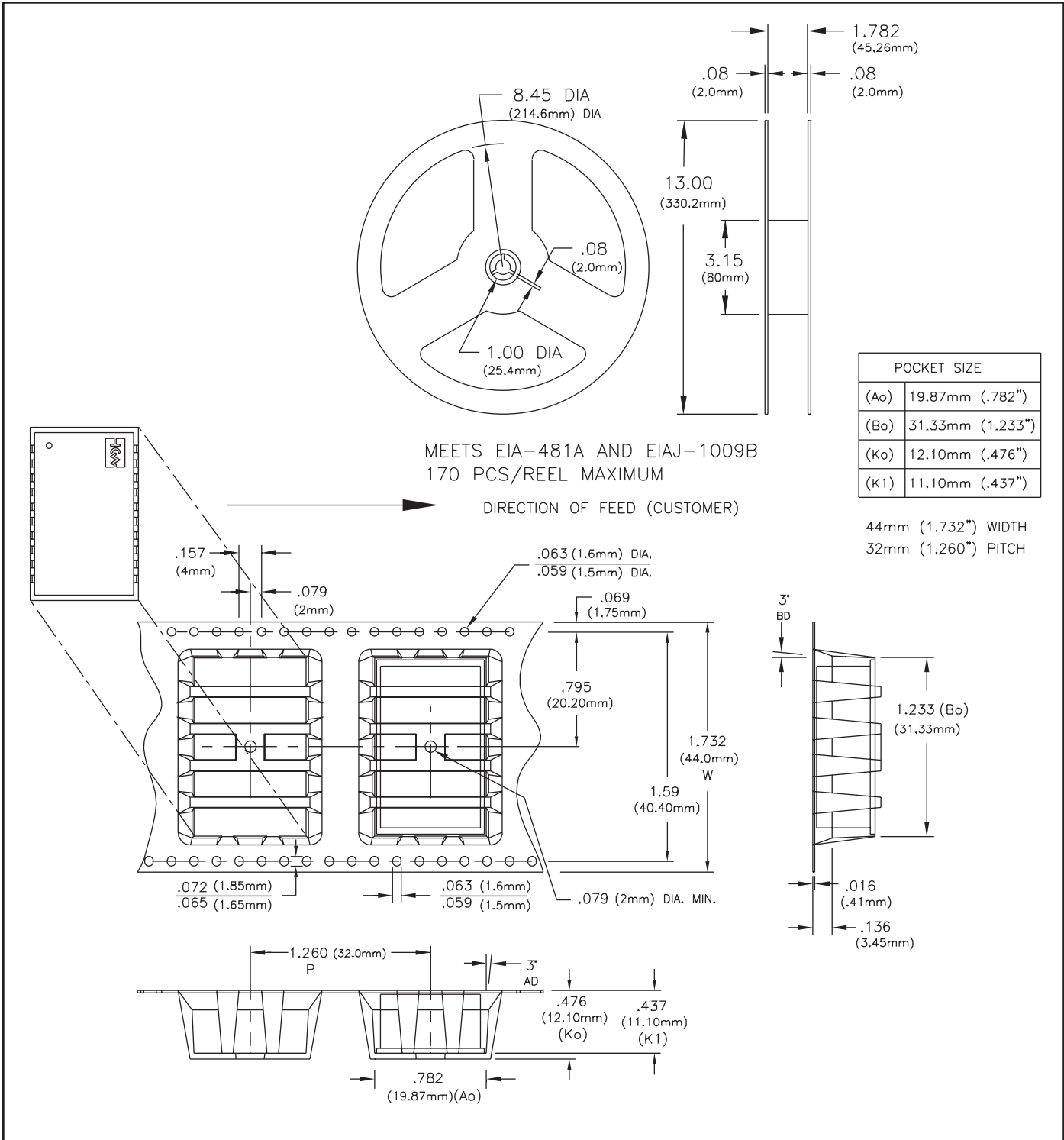
Figure 2





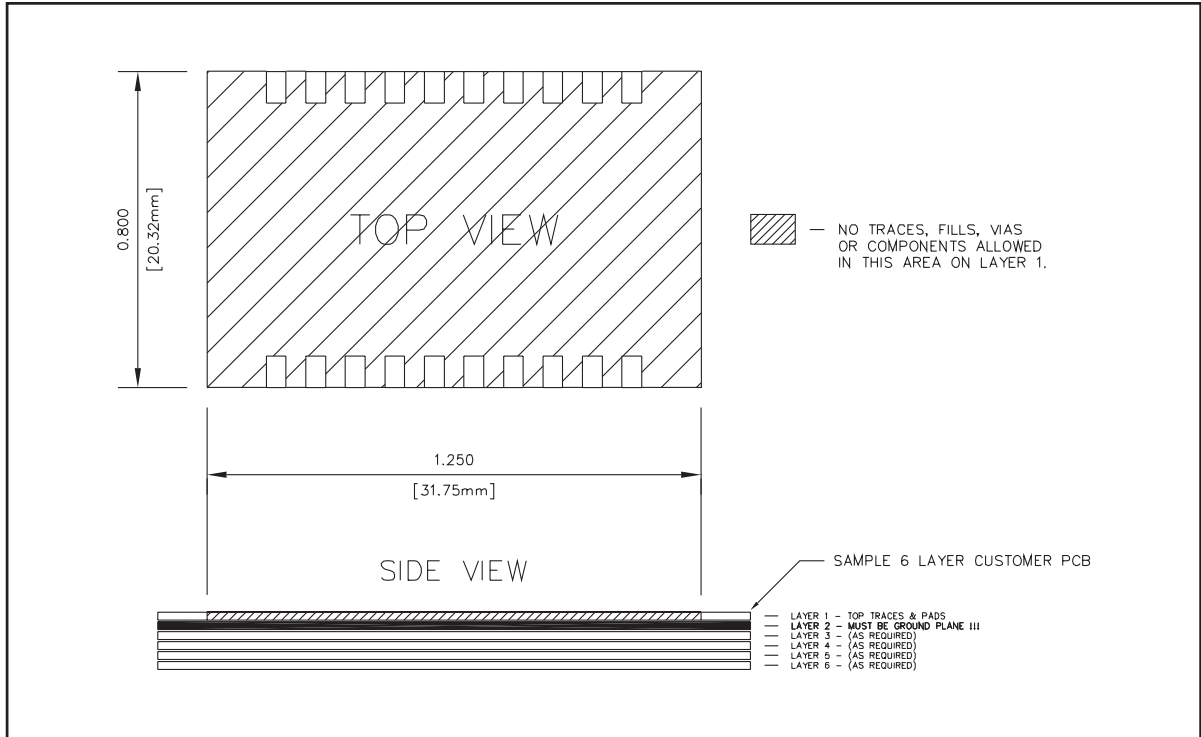
# Tape and Reel Dimensions

Figure 5



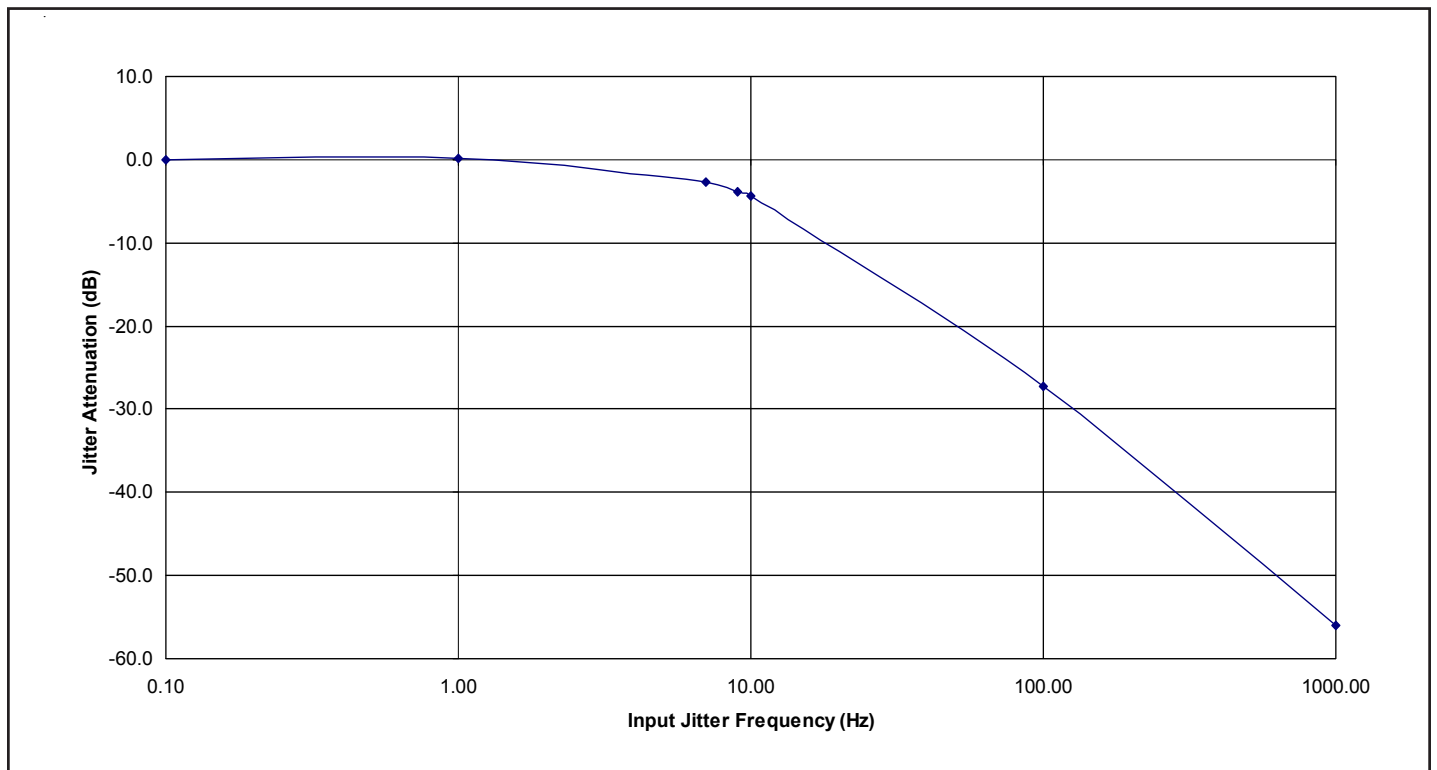
# Recommended Keepout Area & Customer PCB Stackup

Figure 6



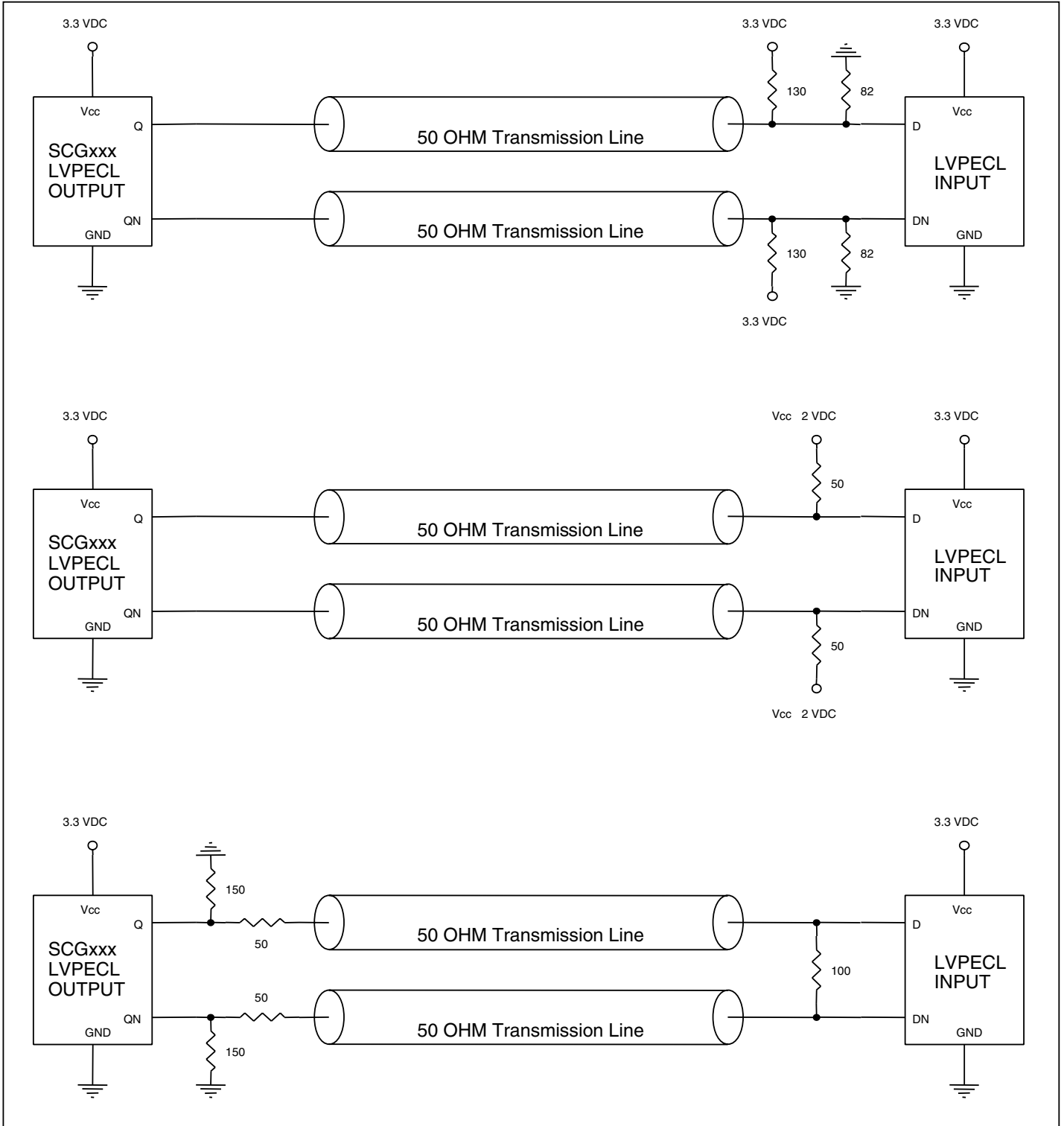
# Jitter Attenuation vs. Input Jitter Frequency

Figure 7



# Recommended LVPECL Termination

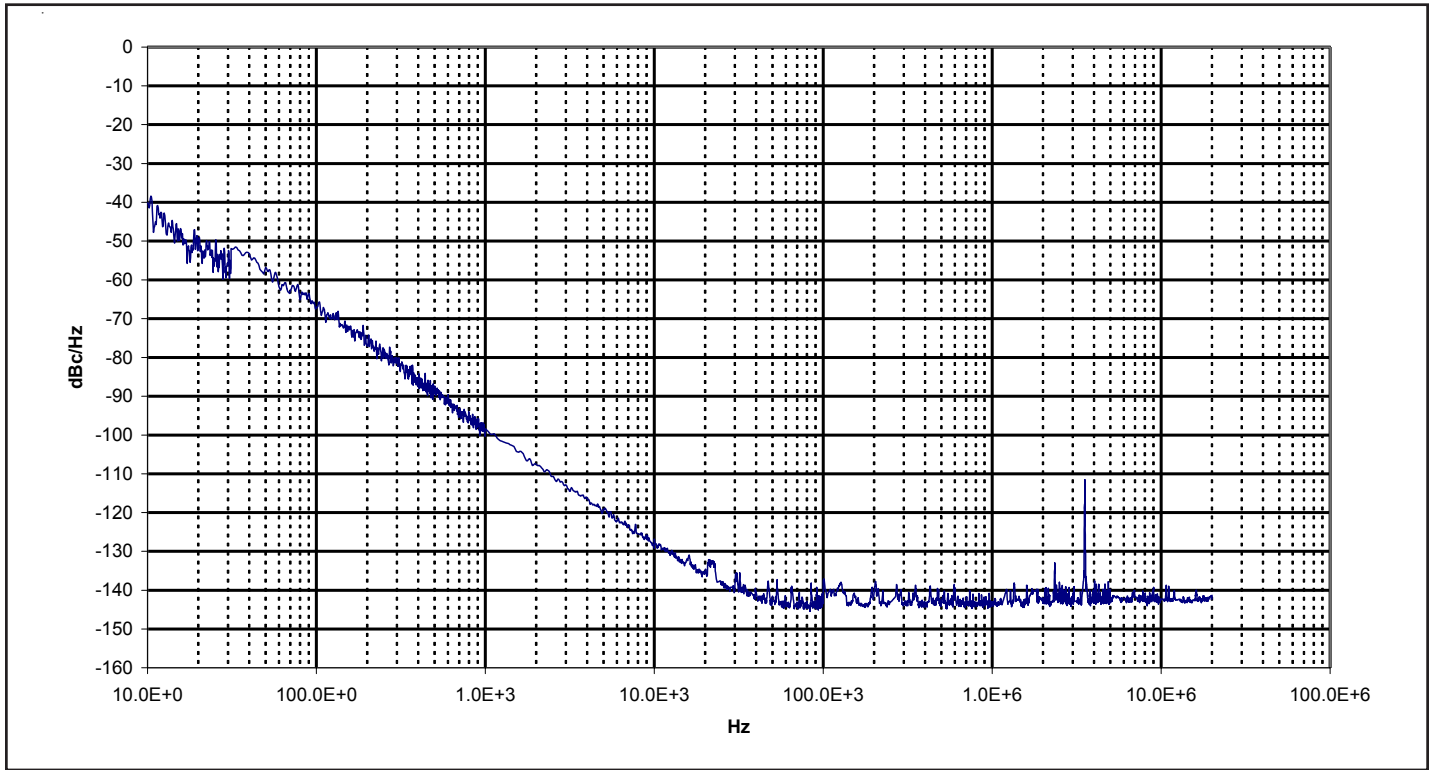
Figure 8



NOTES: 9: Q & QN are differential open emitter outputs

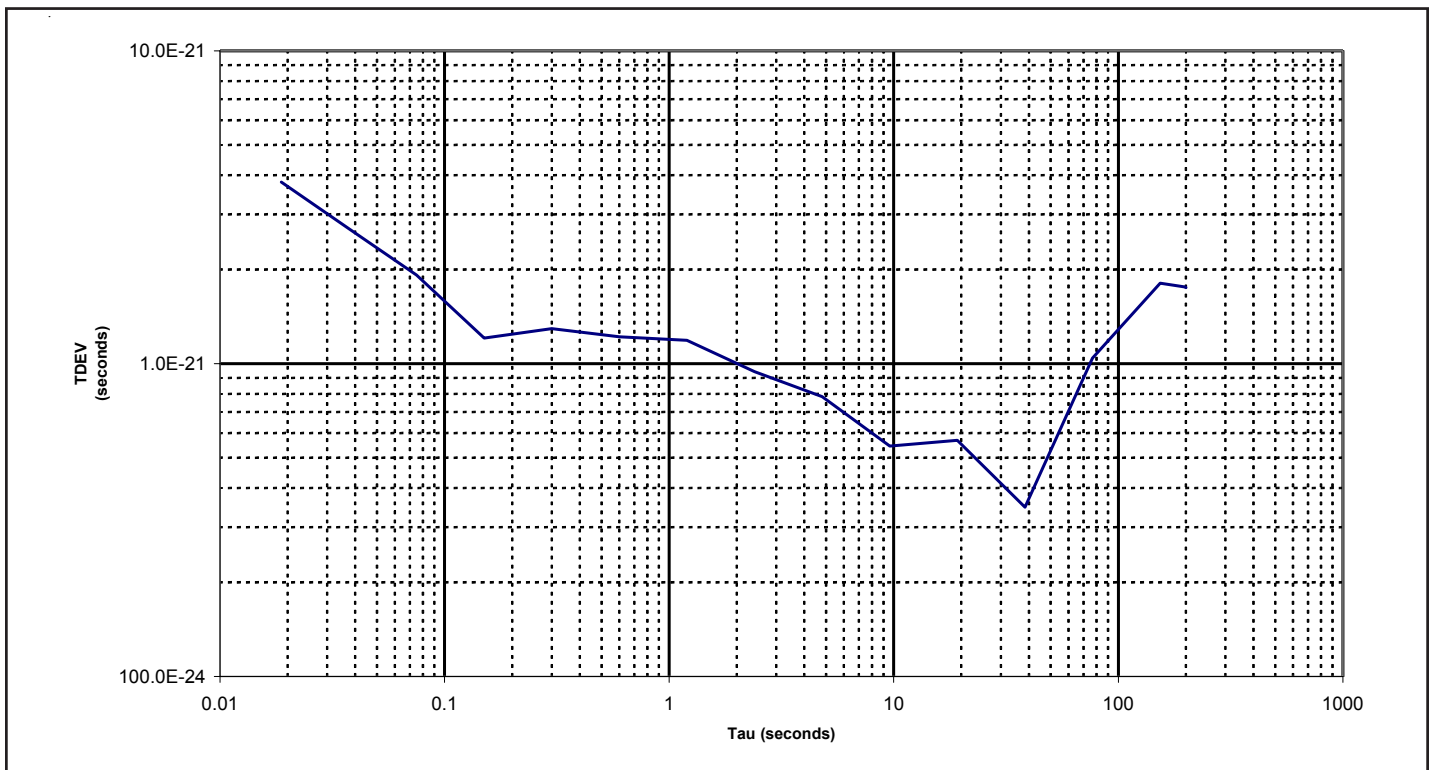
## Typical Phase Noise Plot - Q1, Q2

Figure 9



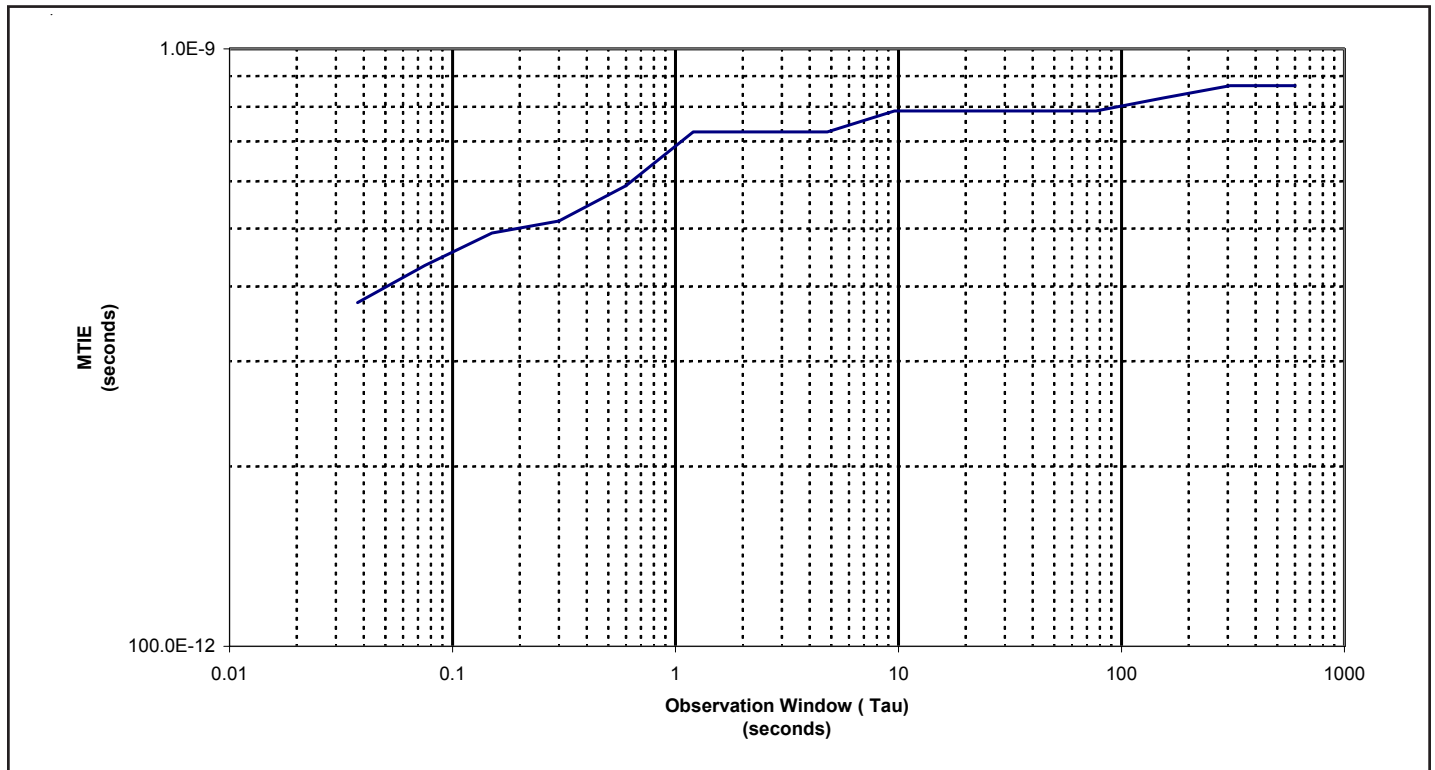
## Typical TDEV Plot

Figure 10



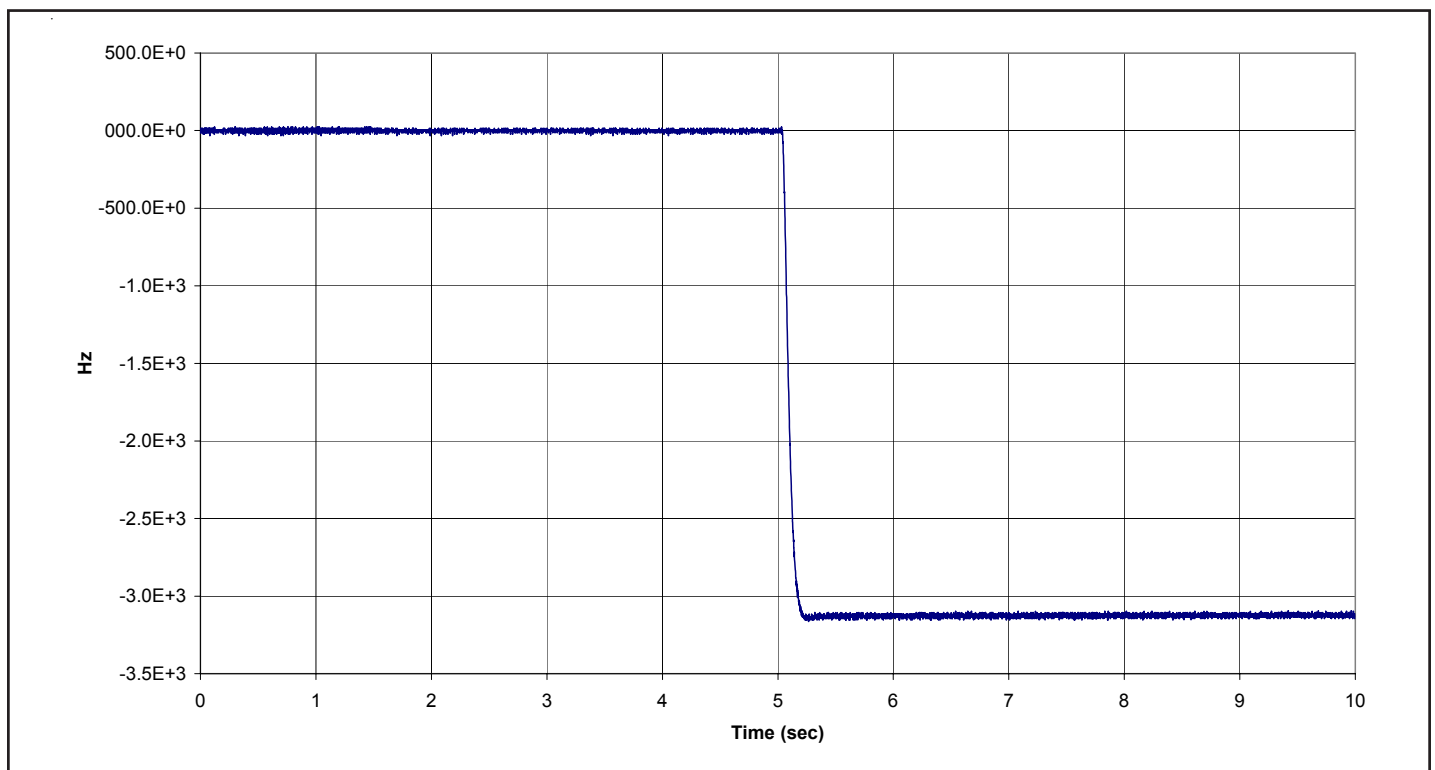
## Typical MTIE Plot

Figure 11



## Typical Step Response due to a 20ppm Frequency Step - Q1, Q2

Figure 12



<b>Revision</b>	<b>Revision Date</b>	<b>Note</b>
P00	2/14/02	Preliminary Informational Release
P01	11/4/02	Updated mech. dimensions & Output specs.

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