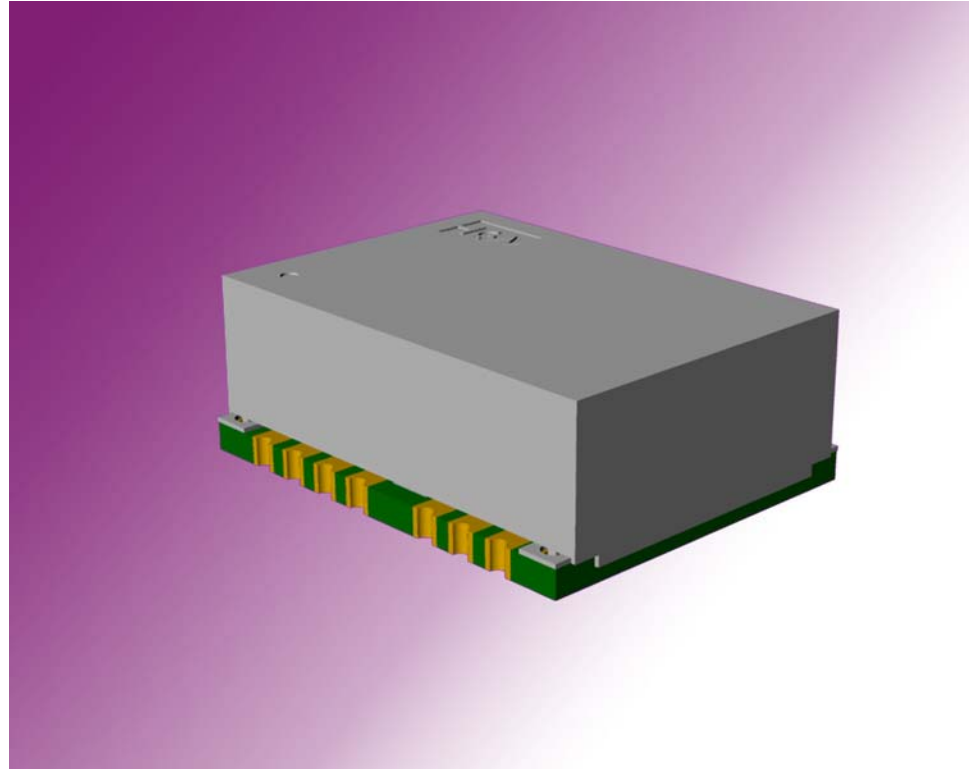


SCG102 Synchronous Clock Generators

PLL

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Application

The Connor-Winfield SCG102 is a 3.3V frequency translator based on a high frequency, crystal oscillator that is input duty cycle tolerant. The SCG102 accepts one input which may be controlled to accept up to four unique reference frequencies between 8 kHz to 170 MHz. The reference frequency selection is controlled by two input select pins.

The SCG102 locks to the input reference and provides a phase-locked output at customer specified frequencies ranging from 77.76 MHz to 170 MHz. The differential output is LVPECL.

Features

- 3.3V High Precision PLL
- Tri-State Capability
- Input Reference Detector
- User Determined Input Reference
- 77.76 MHz to 170 MHz Output Frequencies Available

General Description

The SCG102 provides high precision phase lock loop frequency translation for the telecommunication applications. The SCG102 product generates LVPECL outputs from an intrinsically low jitter, voltage controlled crystal oscillator.

SCG102 is well suited for use in line cards, service termination cards and similar functions to provide reliable reference, phase locked, synchronization for TDM, PDH, SONET and SDH network equipment. The SCG102 provides a jitter filtered, low phase gain (<0.2 dB), wander following output signal synchronized to a superior Stratum or peer input reference signal.

The SCG102 includes the following features: Tri-state and an alarm output for Loss-of-Reference, (LOR), Loss-of-Lock, (LOL). The LVPECL outputs may be put into the tri-state high impedance condition for external testing purposes by asserting a high signal

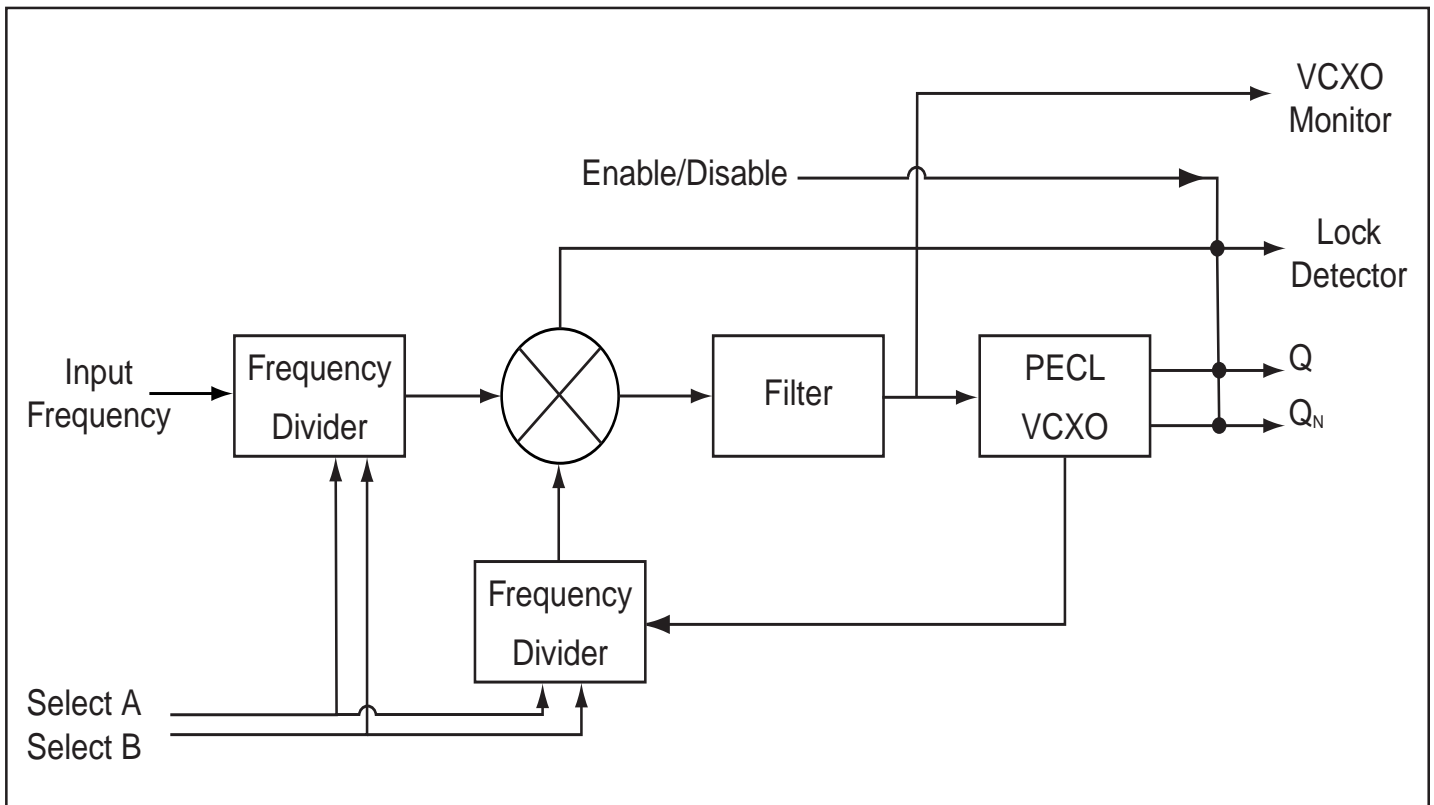
to the Enable/Disable pin.

The SCG102 is a 3.3 Volt component that is estimated to draw between 100 mA and 150 mA. All models have a fast acquisition time of approximately 1 second and can be used in applications that require temperature rating of -40°C - 85° C. The SCG102 package typical dimensions are 1.025" x .80" x .375" (See fig. 2 for maximum dimensions). Parts are assembled using high temperature solder to withstand surface mount reflow process.

The SCG102 locks to any one of four input reference frequencies. The unit may have up to four different frequencies as long as all frequencies are evenly divisible by 8 kHz. The output may be any single frequency from 77.76 MHz to 170 MHz.

Functional Block Diagram

Figure 1



Absolute Maximum Rating

Table 1

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
Vcc	Power Supply Voltage	-0.5		4	Volts	
V1	Input Voltage	-0.5		5.5	Volts	
Ts	Storage Temperature	-65		150	°C	

Specifications

Table 2

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
V _{CC}	Supply Voltage	3.3 - 5%	3.3	3.3 + 5%	Volts	
I _{CC}	Supply Current		150	200	mA	
f _{IN}	Input Frequencies(HCMOS/LVHCMOS)	8 k		170 M	Hz	
f _{OUT}	Output Frequencies(LVPECL)	77.76 M		170 M	Hz	
DC	Positive Duty Cycle	45		55	%	
T _R /T _F	Rise/Fall Time			1	ns	
APR	Input Frequency Tracking	±32			ppm	
BW	Bandwidth			10	Hz	
J _{GEN}	Jitter Generation RMS (12 kHz - 20 MHz)		0.5	1	ps	
J _{TRAN}	Jitter Transfer			0		1
J _{TOL}	Jitter Tolerance					
	8 kHz References	≥31.35			μs	2
	19.44 MHz References	>1			μs	2
Φ	Phase Gain			0.2 dB @-0.1	Hz	
T _{OP}	Operating Temperature	-40		85	°C	
T _{AQ}	Acquisition Time	Apprx. 1 sec. frequency lock when reference is stepped ±10ppm. < 1 sec. phase lock when switching between same frequency references. 30 - 60 sec. phase lock during start-up or when locking from Free Run.				

NOTES: 1.0: All jitter is attenuated (≥10 Hz)

2.0: Jitter transfer refers to the magnitude of input jitter tolerance that results in an alarm.

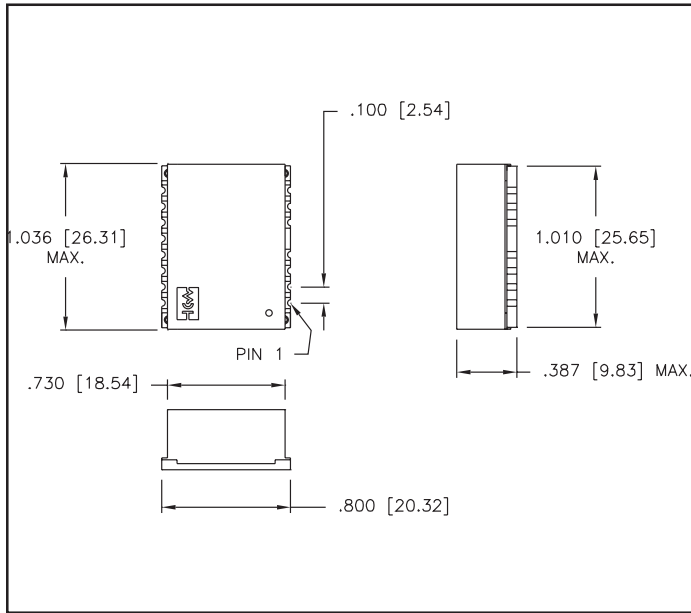
Pin Description

Table 3

Pin #	Connection	Description
1	Reference Input	Reference Input
2	GND	Ground
3	Lock Detector	Logic "1" indicates that the unit is locked to the input reference Logic "0" indicates that the unit is has lost its reference Pulsing indicates that the unit is no longer locked to a reference.
4	VCXO Monitor	Control voltage level for the PECL oscillator
5	----	Missing
6	NC	No connection
7	GND	Ground
8	Enable/Disable	Logic "0" = output enabled
9	Q	LVPECL output
10	Q _N	LVPECL complementary output
11	NC	No connection
12	Input Freq. Select A	Control pin A used to select input frequency. Input is pulled to GND.
13	Input Freq. Select B	Control pin B used to select input frequency. Input is pulled to GND.
14	NC	No connection
15	GND	Ground
16	V _{CC}	Power supply voltage (3.3 Vdc ± 5%)

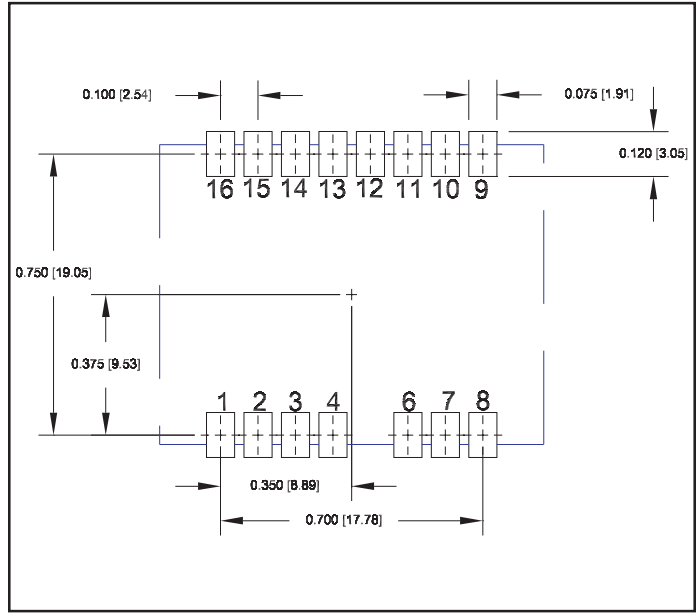
Package Dimensions

Figure 2



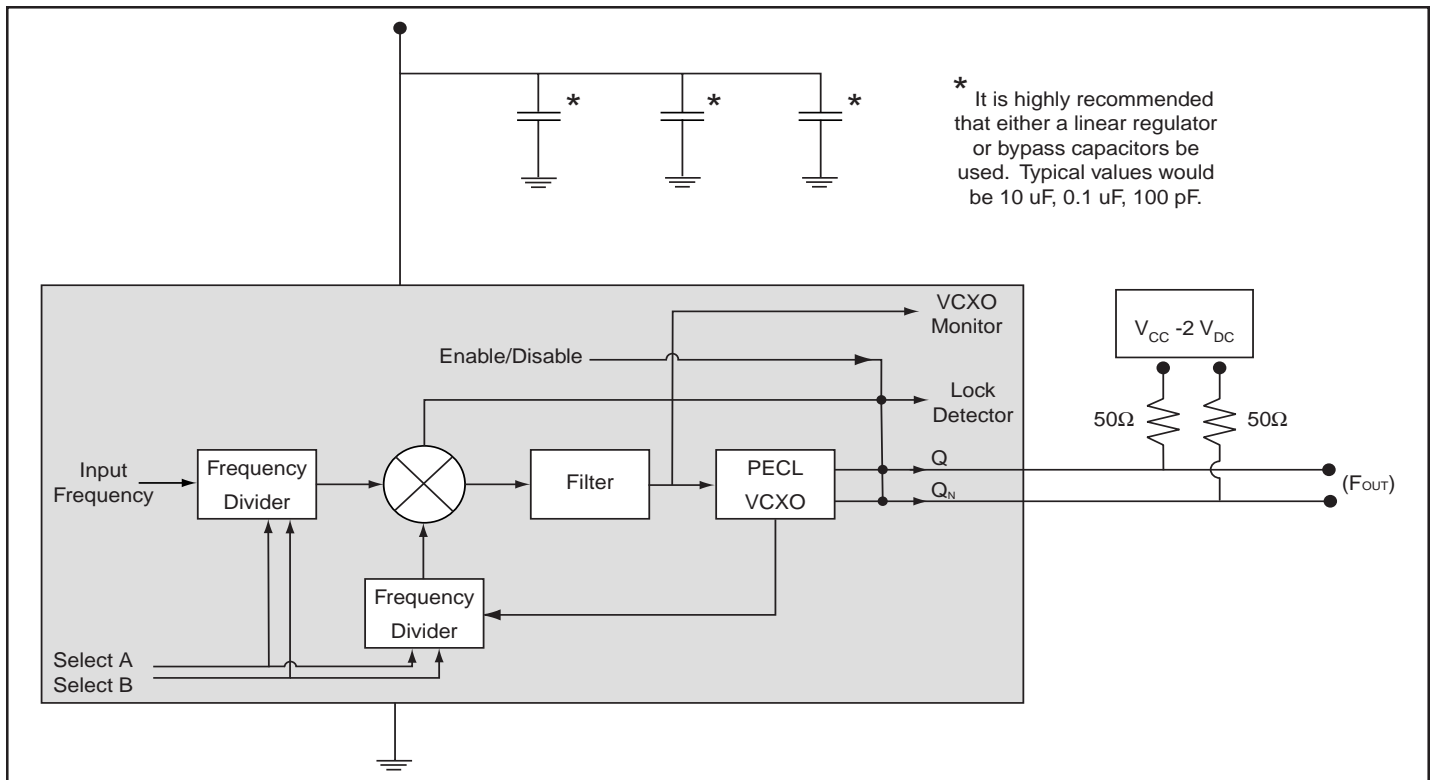
Recommended Footprint Dimensions

Figure 3



Output Load and Power Supply Filtering Recommendations

Figure 4



Ordering Information

10 kHz	B	2.048 MHz	J	51.84 MHz	1
8 kHz	C	6.48 MHz	K	77.76 MHz	2
16 kHz	D	16.384 MHz	N	125.00 MHz	5
64 kHz	E	19.44 MHz	P	155.52 MHz	6
32 kHz	F	20.48 MHz	R	166.6286 MHz	7
1.048 MHz	G	38.88 MHz	X	114.0 MHz	8
1.544 MHz	H	44.736 MHz	Y		

SCG-102- **D** **F** **F** - **A** **1** **P** **6**

Supply Voltage

D = 3.3 V_{DC} ± 5%

Output Type

F = Comp. PECL

Temperature Range

C = 0°C to 70°C

F = -40°C to 85°C

Output Frequency (2 to 8)

See chart above.

Contact a sales representative for the availability of custom frequencies.

Input Frequency (B to 8)

See chart above.

If more than one frequency is desired, enter **S** and list all desired frequencies. Contact a sales representative for the availability of custom frequencies.

Number of Input Frequencies

1 = 1 Input Frequency

2 = 2 Input Frequencies

3 = 3 Input Frequencies

4 = 4 Input Frequencies

Input Logic

A = CMOS

Sample Part Number Examples:

SCG-102- DFF-A1C2

SCG-102- DFF-A4S2, S = 8 kHz, 16.384 MHz, 19.44 MHz, 38.88 MHz





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Revision	Revision Date	Note
A00	3/4/02	Advance Informational Release
A01	1/28/03	Added new frequencies (K, G)
A02	7/17/03	Added new frequencies (B, 8)