SCG2500A Synchronous Clock Generator

CONNOR WINFIELD

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General Description

The SCG2500A is a mixed-signal phase lock loop generating CMOS outputs from an intrinsically low jitter voltage controlled crystal oscillator. The SCG2500A is based on Connor-Winfield's SCG2500 series product line.

The SCG2500A can lock to one of two possible reference inputs at 8 kHz that are selectable using one input select pin. The SCG2500A has an improved filter compared to the SCG2500. The new filter allows the SCG2500A to more closely track the selected input reference and lowers switching MTIEs.

The SCG2500A provides 3 alarm outputs, Loss of Reference A, (LOR A) Loss of Reference B, (LOR B), and Loss of Lock, (LOL) as compared to the SCG2500's combined alarms. In the event of a LOL condition, the LOL alarm will activate in 1us of the next rising edge of the internal, 8 kHz reference. Switching references within 100 ns will then comply with GR-253-CORE requirements. LOR A and LOR B independently monitor the input references. If Both references are lost the unit will go into Free Run automatically. When both references are lost, the unit should be forced into Free Run (pin 5 = 1). LOR A and LOR B can then be monitored until the references return. Refer to Table 6 for more operational details.

The reference output at 8 kHz is derived from the oscillator output. Note that the offset between the filtered output and the reference input will change with each reference rearrangement.

The package maximum dimensions are .780" x .830" x .350" on a six layer FR4 board with surface mount pins. Parts are assembled using high temperature solder to withstand surface mount reflow processes.

Tri-State is not available with this model.

Features

- Phase Locked Output Frequency Control
- Intrinsically Low Jitter Crystal Oscillator
- Two Selectable References @ 8 kHz
- Hitless Reference Switching
- 2 Independent Reference Monitors
- LOL Alarm Output
- Force Free Run Function
- Automatic Free Run Operation upon loss of both references
- Input Duty Cycle Tolerant
- 3.3 Volt Power Supply
- Small Size: 0.78" x 0.83" x 0.35" maximum
- Surface Mount, DIL Package

Quick Overview		
Ref_In	**Osc_Out**	**Ref_Out**
8 kHz	2.048 MHz	8 kHz
8 kHz	19.44 MHz	8 kHz
8 kHz	51.84 MHz	8 kHz
8 kHz	77.76 MHz	8 kHz

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630-851-4722
European Headquarters:
+353-61-472221

Absolute Maximum Rating

Table 1

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
V_{CC}	Power Supply Voltage	-0.5	-	+4.0	Volts	
V_I	Input Voltage	-0.5	-	+5.5	Volts	
T_S	Storage Temperature	-65.0	-	+150.0	°C	

Operating Specifications

Table 2

Parameter	Specifications	Notes
Voltage	3.3V ±5%	1.0
Current	150 mA @ 3.46V	
Input Frequency Ref 1 and Ref 2	8 kHz	2.0
Available Oscillator Output Frequencies	2.048,19.44 MHz, 51.84 MHz, 77.76 MHz	
Reference Output	8 kHz	
Temperature Range	0 to 70°C	
Input Jitter Tolerance *(Jitter Frequencies ≥ 10 Hz)*	≥ 1us Typical	
Jitter Bandwidth	< 10 Hz	
Acquisition Time	Apprx. 1 sec. frequency lock when reference is stepped up or down 10ppm < 1 sec. phase lock when switching between same frequency references 30 - 60 sec. phase lock during start-up or when locking from Free Run	
Capture/Pull-In Range	± 25 ppm Minimum	
Output Duty Cycle	40/60 % Min/Max @ 50% Level	
Output Rise and Fall Time	3 nS @ 20% to 80% output level	
Output Load	30 pF	
Alarm	LOR A, LOR B, LOL	
Free Run Accuracy	±20 ppm	
Package	Fr4 SM 0.78” x 0.83” x 0.350” (Maximum)	
MTIE @ Synchronization Rearrangement	GR-253-CORE, 1999 R5-136	4.0, 4.1
Static Offset	± 19 ns	6.0
Dynamic Offset	± 13 ns	

Input and Output Characteristics

Table 3

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
V_{IH}	High level input voltage	2.0	-	5.5	V	
V_{IL}	Low level input voltage	0	-	0.8	V	
T_{IO}	I/O to output valid	-	-	10	nS	
C_{OUT}	Output capacitance	-	-	10	pF	
V_{HO}	High level output voltage Ioh = -4mA	2.40	-	-	-	Vcc Min
V_{IO}	Low Level output voltage Io1 = 8mA	-	-	0.4	-	Vcc Max
T_{IR}	Input reference signal pulse width	30	-	-	nS	

Output Jitter Specifications

Table 4

Frequency (MHz)	Jitter BW 10 Hz - 20 MHz pS (RMS)	m UI	SONET Jitter BW 12 kHz - 20 MHz pS (RMS)	m UI
2.048	30 Typ.	0.061 Typ.	3 Typ.	0.006 Typ.
19.44	10 Typ.	0.194 Typ.	1 Max., 0.5 Typ.	0.019 Max.
51.84	10 Typ.	0.518 Typ.	1 Max., 0.5 Typ.	0.052 Max.
77.76	10 Typ.	0.777 Typ.	1 Max., 0.5 Typ.	0.077 Max.

Operational Table

Table 5

INPUTS				**OUTPUTS**				
Select A/B	Ref A	Ref B	Force Free Run	Oscillator Output	Ref Out	LOL	LOR A	LOR B
X	A	A	1	FR	FR	0	1	1
X	NA	A	1	FR	FR	0	0	1
X	A	NA	1	FR	FR	0	1	0
X	NA	NA	0 **	FR	FR	0	0	0
0	A	A	0	RA	RA	1	1	1
0	A	NA	0	RA	RA	1	1	0
0	NA	A	0	U	U	0	0	1
1	A	A	0	RB	RB	1	1	1
1	NA	A	0	RB	RB	1	0	1
1	A	NA	0	U	U	0	1	0

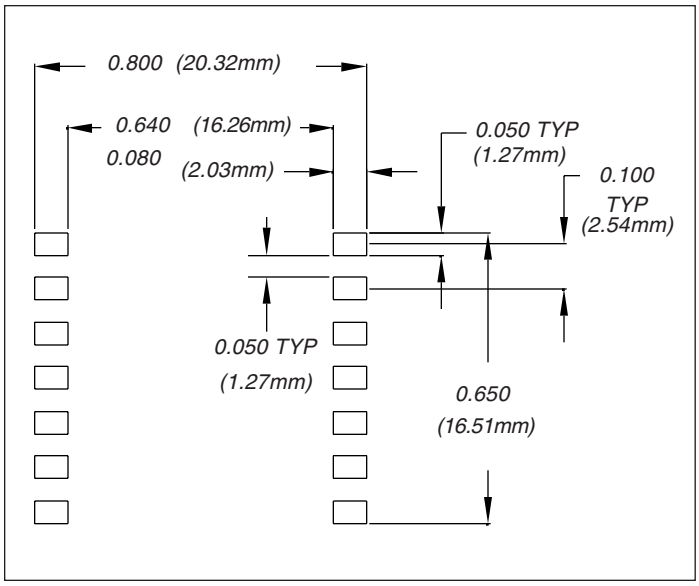
Notes:
A = Active
NA = Not Active
FR = Free Run
RA = Locked to Reference A
RB = Locked to Reference B
U = Unstable (See note 7)
X = Don't Care
** See Note 8.0

NOTES:

1.0 Requires external regulation
2.0 Externally selectable via Input Select AB
3.0 From a 20 ppm offset in reference frequency
4.0 Entry into Free Run doesn't meet requirement for initial 2.33 seconds of self-timing
4.1 If the selected reference is removed, system response to the LOL ALARM must be less than 100ns
5.0 Upon power-up, allow 60 seconds for the SCG to obtain tight phase lock.
6.0 Static offset will accumulate with each reference switch for the Reference Output only.
7.0 Frequency will drift to lower limit rail if not switched.
8.0 Loss of both references will automatically force Free Run. Change the Force Free Run (pin 5) to 1 upon detection of this condition.

Circuit Board Footprint

Figure 1



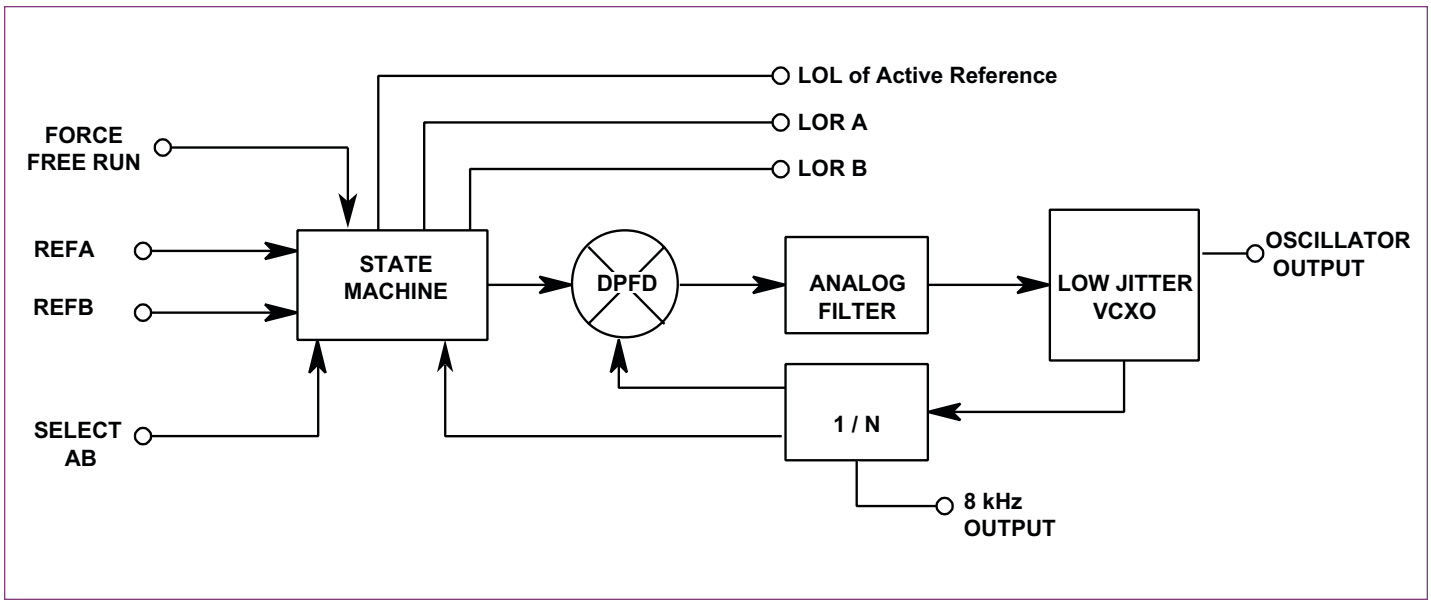
Pin Connections

Table 6

Pin	Connection
1	Filtered 8 kHz Output
2	TCK (Do not connect, Factory use only)
3	TMS (Do not connect, Factory use only)
4	Ground
5	Force Free Run / TDI (1 = Free Run)
6	LOR A (1=Active Reference, 0=LOR)
7	REF B
8	REF A
9	Oscillator Output
10	LOR B (1=Active Reference, 0=LOR)
11	Vcc
12	TDO (Do not connect, Factory use only)
13	LOL of active reference (1=Locked, 0=Unlocked)
14	Input Reference Select AB (A = 0, B = 1)

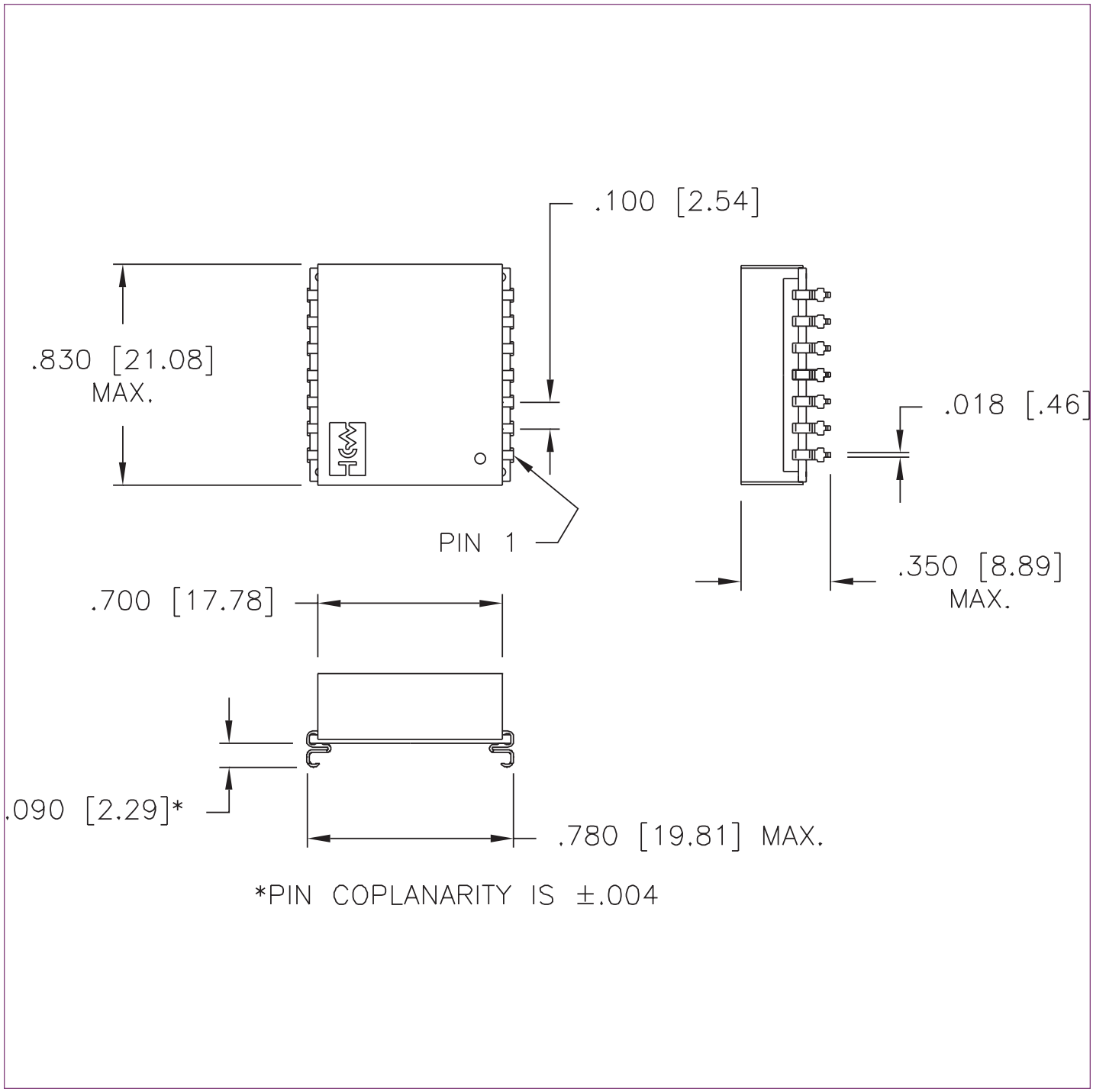
Block Diagram

Figure 2



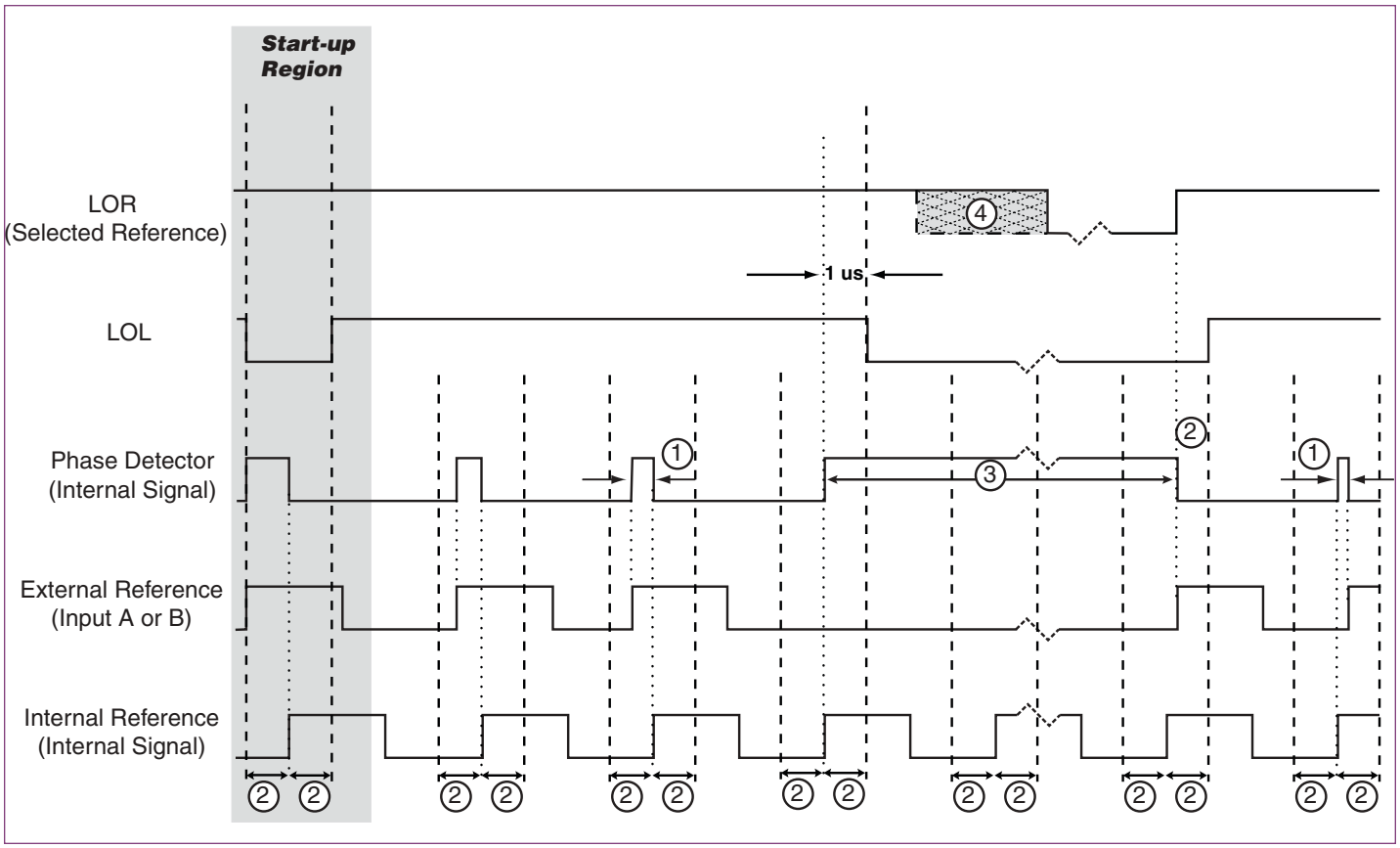
Package Maximum Dimensions

Figure 3



LOR Alarm Diagram

Figure 4



AlarmTiming Legend

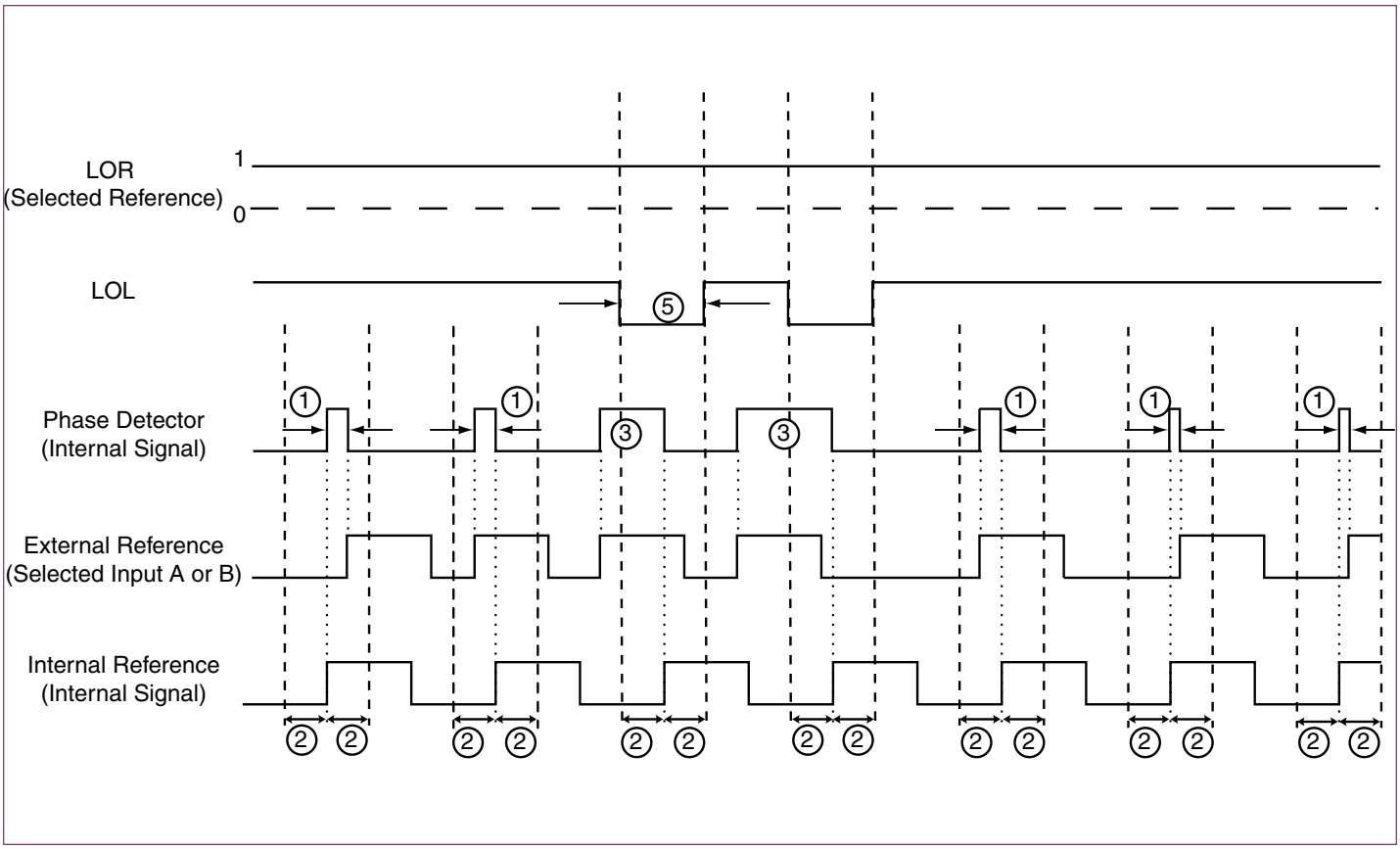
Use for all alarm timing diagrams

Table 7

	8 kHz Reference Input
1	< 1 µsec
2	1 µsec
3	> 1 µsec
4	124 µsec(min) to 374 µsec(max) after LOL
5	Minimum pulse width = 2 µs
Start-up Region	During Start-up, The LOL Alarm will pulse during the few seconds of operation

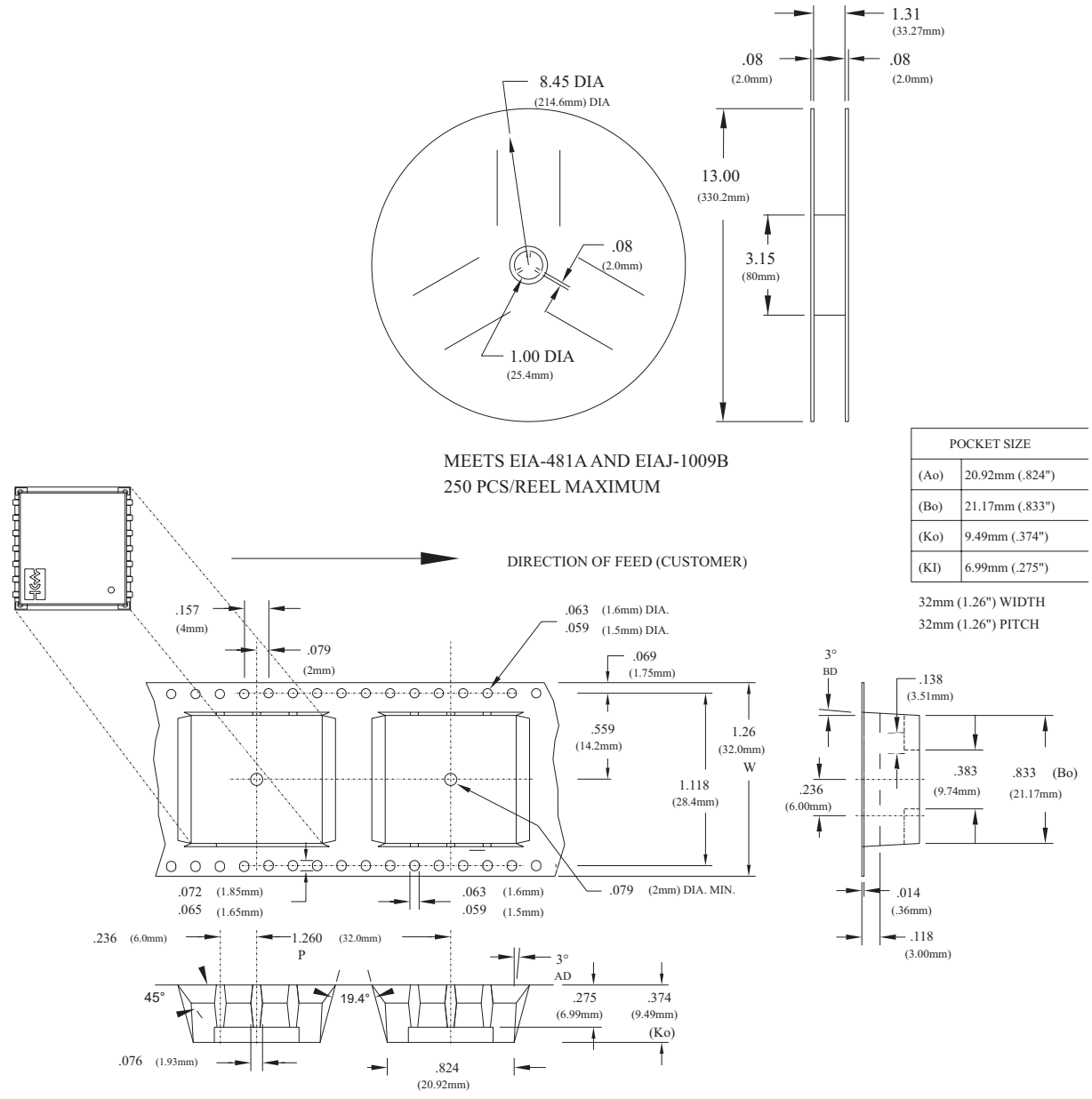
LOL Alarm Diagram

Figure 5



Tape and Reel Packaging

Figure 6

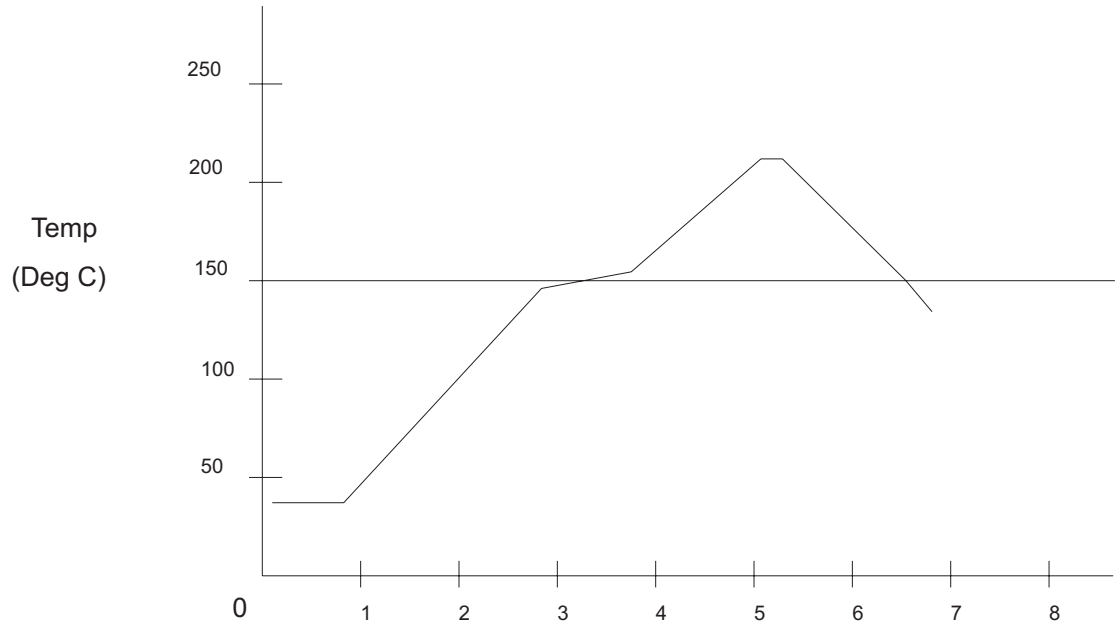


POCKET SIZE	
(Ao)	20.92mm (.824")
(Bo)	21.17mm (.833")
(Ko)	9.49mm (.374")
(KI)	6.99mm (.275")

32mm (1.26") WIDTH
32mm (1.26") PITCH

Solder Profile

Figure 7



Recommended Reflow Profile

Peak Temp:	217 Deg C
Max Rise Slope:	1.5 Deg C/Sec
Time Above 150 C:	100 Sec

Ordering Information

SCG{XXXX}-{FFF.FFF}{M}

XXXX equals a specific model (2500A)
FFF.FFF equals the Oscillator Output frequency (002.048, 019.44, 051.84, or 077.76)
M equals MHz and is added to all part numbers

Example: To order an SCG2500A with an Oscillator Output of 19.44 MHz,
Order part number SCG2500A-019.44M

Please contact Connor-Winfield for other frequencies that may be available.

Revision	Revision Date	Note
A00	5/17/02	Advance Informational Release
A01	6/12/02	Revised for design changes
A02	6/27/02	Changed pg.1 picture
A03	2/18/03	Added 51.84 MHz
A03	4/26/04	Added 2.048
MHz		