SCG4505 Synchronous Clock Generators

PLL

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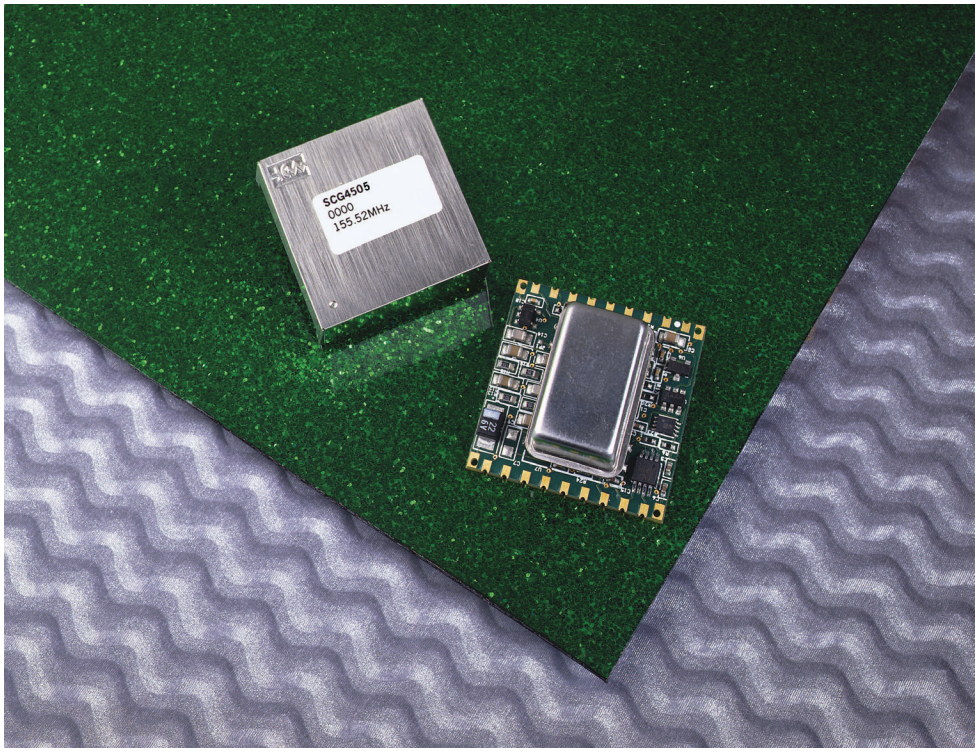


Features

- LVPECL Output Frequencies @ 155.52 MHz or 77.76 MHz
- CMOS Output Frequency @ 77.76 MHz
- Phase Locked Output Frequency Control
- Intrinsically Low Jitter Crystal Oscillator
- LVPECL Outputs with Disable Function
- Dual Input References
- LOR & LOL combined alarm output
- Force Free Run Function
- Automatic Free Run operation on loss of both References A & B
- Input Duty Cycle Tolerant
- 3.3V dc Power Supply
- Small Size: 1 Square Inch

Bulletin	**SG058**
Page	**1 of 16**
Revision	**P01**
Date	**31 JAN 03**
Issued By	**MBatts**

General Description

The SCG4505 is a mixed-signal phase locked loop generating LVPECL outputs from an intrinsically low jitter, voltage controlled, crystal oscillator. The LVPECL outputs may be disabled. The SCG4505 also provides a CMOS Output @ 77.76 MHz on the REF_OUT pin.

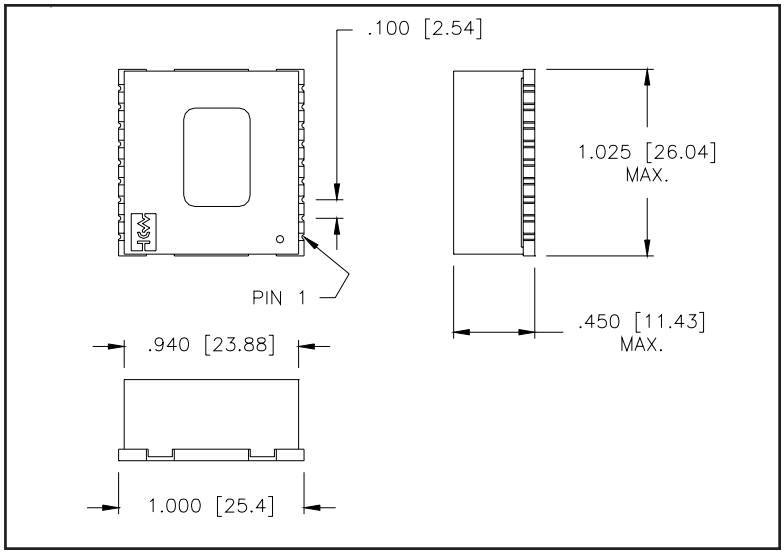
The SCG4505 can lock to one of two external references, which is selectable using the SEL_{AB} input select pin. The unit has a fast acquisition time of about 1 second and it is tolerant of different reference duty cycles.

The SCG4505 includes an alarm output that indicates deviations from normal operation. If a Loss-of-Reference (LOR) or Loss-of-Lock (LOL) is detected the alarm with indicate the need for a reference rearrangement. If both references A and B are absent the module will enter Free Run operation. The FR_{status} pin will indicate that the module is in Free Run operation. Frequency stability during Free Run operation is guaranteed to ±20 ppm. Additionally the Free Run mode may be entered manually.

The package dimensions are 1.00" x 1.025" x 0.45" on a 6 layer FR4 board with castellated pins. Parts are assembled using high temperature solder to withstand 63/37 alloys, 180°C surface mount reflow processes.

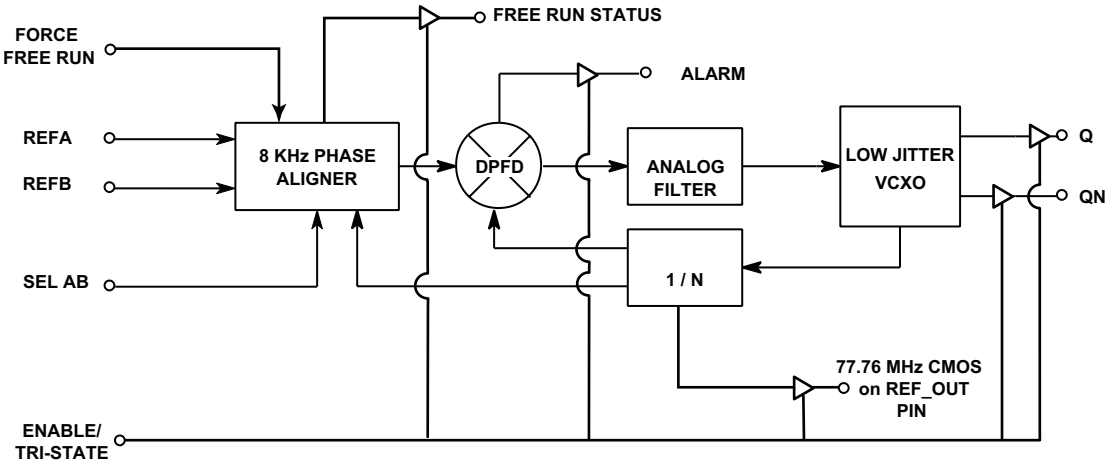
Maximum Dimension Package Outline

Figure 1



Block Diagram

Figure 2



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Absolute Maximum Rating

Table 1

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
V_{cc}	Power Supply Voltage	-0.5	-	+4.0	Volts	1.0
V_i	Input Voltage	-0.5	-	+5.5	Volts	1.0
T_s	Storage Temperature	-65.0	-	+100	°C	1.0

Operating Specifications

Table 2

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
V_{cc}	Power Supply Voltage	3.135	3.3	3.465	Volts	2.0
I_{cc}	Power Supply Current	-	230	-	mA	4.0
T_o	Temperature Range	0	-	70	°C	
f_{in}	Input Frequency	-	8	-	kHz	
f_{out}	LVPECL Synchronized Output Frequency	-	77.76 or 155.52	-	MHz	
f_{ref}	CMOS Output Frequency	-	77.76	-	MHz	
f_{fr}	Free Run Frequency	-20	-	20	ppm	
f_{cap}	Capture/pull-in range	-25	-	25	ppm	
f_{bw}	Jitter Filter Bandwidth	-	-	10	Hz	3.0
t_{jtol}	Input Jitter Tolerance *(Input Jitter Frequencies ≥ 10 Hz)*	1	-	-	µs	
t_{rf}	Output Rise and Fall Time (20% 80%)	100	225	350	ps	4.0
DC	Output Duty Cycle	40	50	60	%	
$MTIE_{sr}$	MTIE at Synchronization Rearrangement		GR-253-CORE.1999 R5-136			5.0, 6.0
t_{aq}	Acquisition Time	Apprx. 1 sec. frequency lock when reference is stepped up or down 10ppm < 1 sec. phase lock when switching between same frequency references 30 - 60 sec. phase lock during start-up or when locking from Free Run				

Output Jitter Specifications

Table 3

Frequency (MHz)	Jitter BW 10 Hz - 1 MHz pS (RMS)	m UI	SONET Jitter BW 12 kHz - 20 MHz pS (RMS)	m UI
LVPECL (Synchronized Output)				
77.76	10 Typ.	0.776 Typ.	1 Max.	0.076 Max.
155.52	10 Typ.	1.556 Typ.	1 Max.	0.156 Max.
CMOS (Filtered Reference Output)				
77.76	25 Typ.	1.944 Typ.	3 Typ.	0.233 Typ.

NOTES:

1.0 Operation of the device at these or any other condition beyond those listed under Operating Specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

2.0 Requires external regulation and supply decoupling. (22 uF, 330 pF)

3.0 3db loop response.

4.0 50-ohm load biased to 1.3 volts.

5.0 Entry into Free Run doesn't meet requirement for initial 2.33 seconds of self-timing.

6.0 If the selected reference is removed system response to the ALARM must be less than 100ns.

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Input And Output Characteristics

Table 4

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
CMOS Input and Output Characteristics						
V_{ih}	High Level Input Voltage	2.0	-	5.5	V	
V_{il}	Low Level Input Voltage	0.0	-	0.8	V	
T_{io}	I/O to Output Valid	-	-	10	ns	
C_l	Output Capacitance	-	-	10	pF	
V_{oh}	High Level Output Voltage	2.4	-	-	V	
V_{ol}	Low Level Output Voltage	-	-	0.4	V	
T_{ir}	Input Reference Pulse Width	12.5	-	-	ns	
LVPECL Output Characteristics						
V_{oh}	High Level PECL Voltage	2.27	2.34	2.52	V	
V_{ol}	Low Level PECL Voltage	1.49	1.51	1.68	V	
C_l	Output Capacitance	-	-	10	pF	
T_{skew}	Differential Output Skew	-	50	-	ps	

Input Selection / Output Response

Table 5

INPUTS						OUTPUTS				NOTE
RESET	**ENABLE**	**SEL_{AB}**	**REF_A**	**REF_B**	**FR**	**FR_{status}**	**ALARM**	**Q**	**QN**	
1	0	X	X	X	X	1	1	X	X	FR
X	1	X	X	X	X	X	X	0	1	
0	0	X	X	X	1	1	1	X	X	FR
0	0	0	A	A	0	0	0	X	X	RA
0	0	1	A	A	0	0	0	X	X	RB
0	0	0	NA	A	0	0	1	X	X	U
0	0	1	NA	A	0	0	0	X	X	RB
0	0	1	A	NA	0	0	1	X	X	U
0	0	0	A	NA	0	0	0	X	X	RA
0	0	X	NA	NA	0	1	1	X	X	FR

NOTES:
A Active
FR Free Run Mode
NA Not Active
RA Locked to Reference A
RB Locked to Reference B
U Unstable (due to conditions shown, switch to active reference or Free Run)
X Don't care

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Pin Description

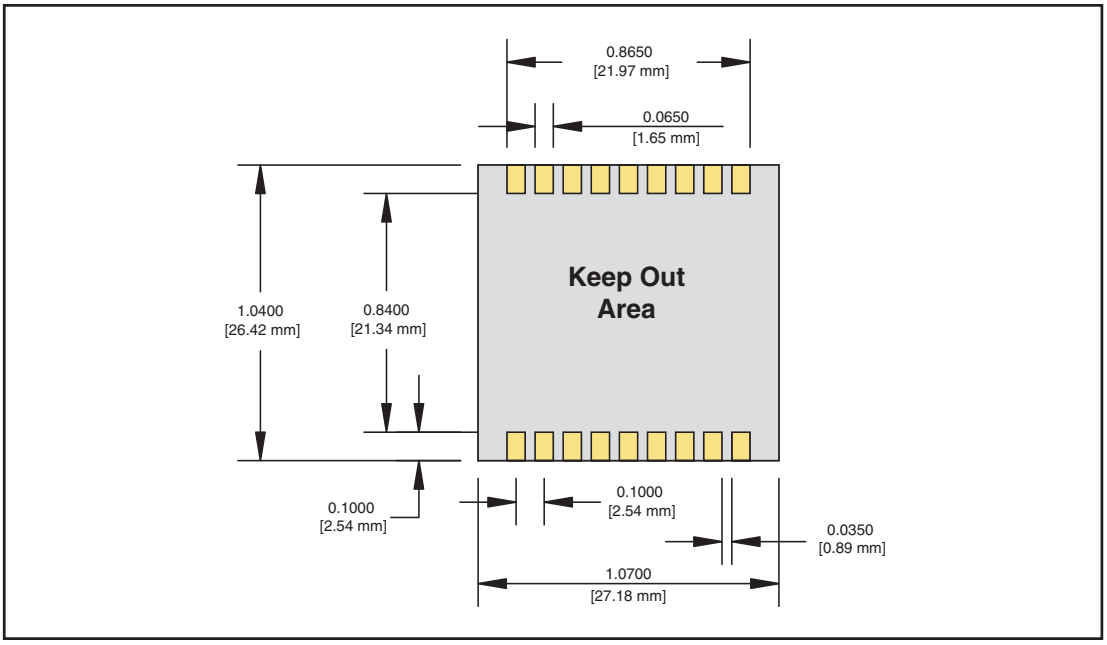
Table 6

Pin #	Pin Name	Pin Information	Note
1	ENABLE/TRI-STATE	VCXO Enable. (Enable = 0, Disable = 1 = CMOS Outputs Tri-stated)	9.0
2	TCK	No Connection, Internal Factory Programming Input.	8.0
3	TDO	No Connection, Internal Factory Programming Input.	8.0
4	REF_A	CMOS Reference Frequency Input.	
5	SEL_{AB}	Input Reference Select Pin. (REFA = 0, REFB = 1)	9.0
6	RESET	RESET. (RESET = 1)	9.0
7	REF_B	CMOS Reference Frequency Input.	
8	V_{ee}	Ground.	
9	FR_{status}	Free Run Status. (FR = 1)	
10	V_{cc}	Supply Voltage relative to ground.	
11	REF_OUT	Filtered 77.76 MHz CMOS output	
12	ALARM	Loss of Reference / Lock alarm. (Alarm = 1)	
13	FR	Force Free Run. (Phase Lock = 0, Free Run = 1)	9.0
14	TDI	No Connection, Internal Factory Programming Input.	8.0
15	TMS	No Connection, Internal Factory Programming Input.	8.0
16	QN	LVPECL Complementary Output.	
17	V_{ee}	Ground.	
18	Q	LVPECL Output.	

NOTES
8.0 Do not connect pin
9.0 Input pulled to ground

Circuit Board Footprint & Keepout Recommendations

Figure 3



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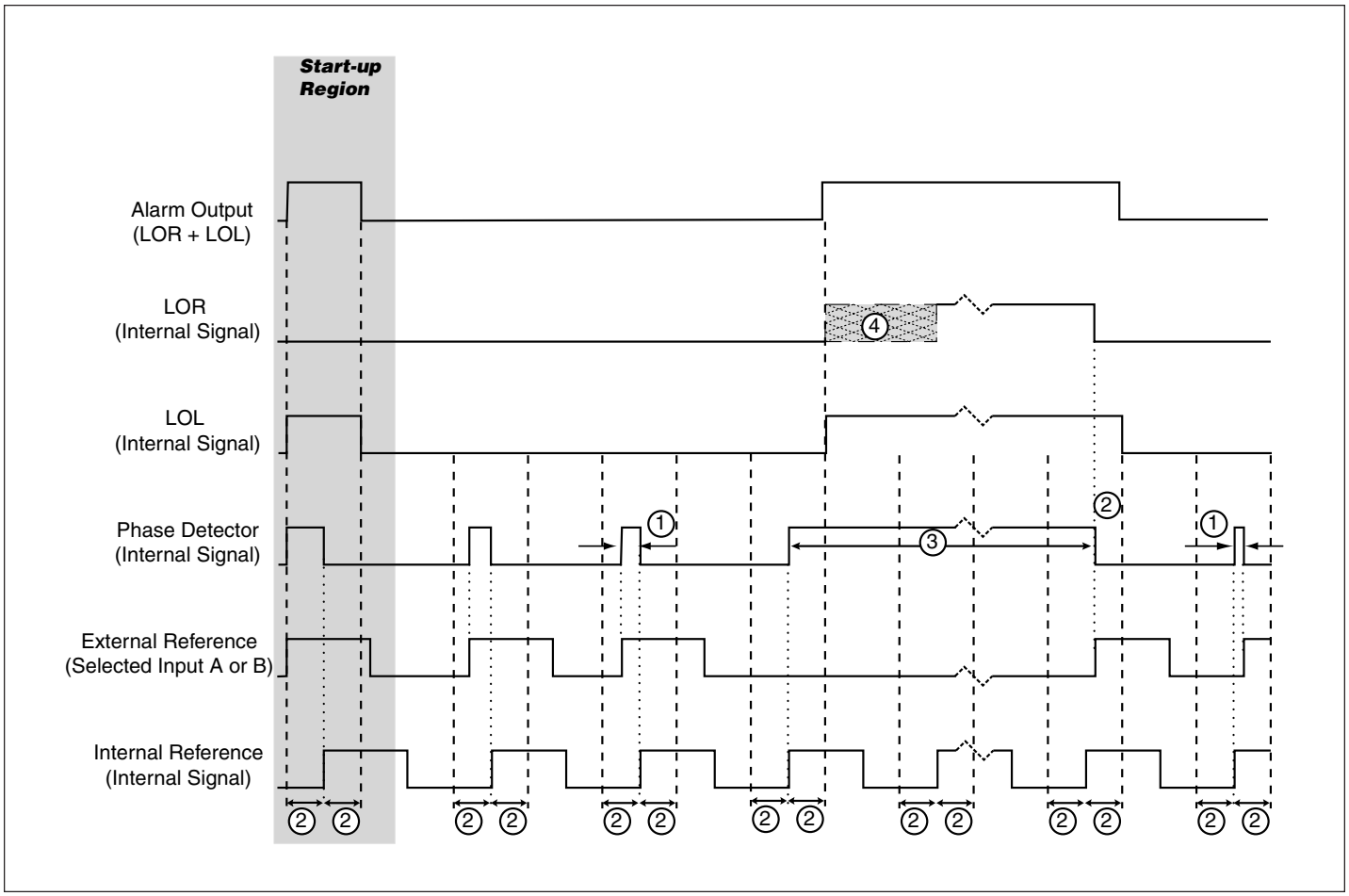
Loss of Reference Condition Alarm Timing

Figure 4



AlarmTiming Legend

Use for all alarm timing diagrams

Table 7

	SCG4505 Alarm Characteristics
1	< 1 µsec
2	1 µsec
3	> 1 µsec
4	124 µsec(min) to 374 µsec(max) after LOL
5	Minimum pulse width = 2 µs
Start-up Region	During Start-up, The LOL Alarm will pulse during the few seconds of operation

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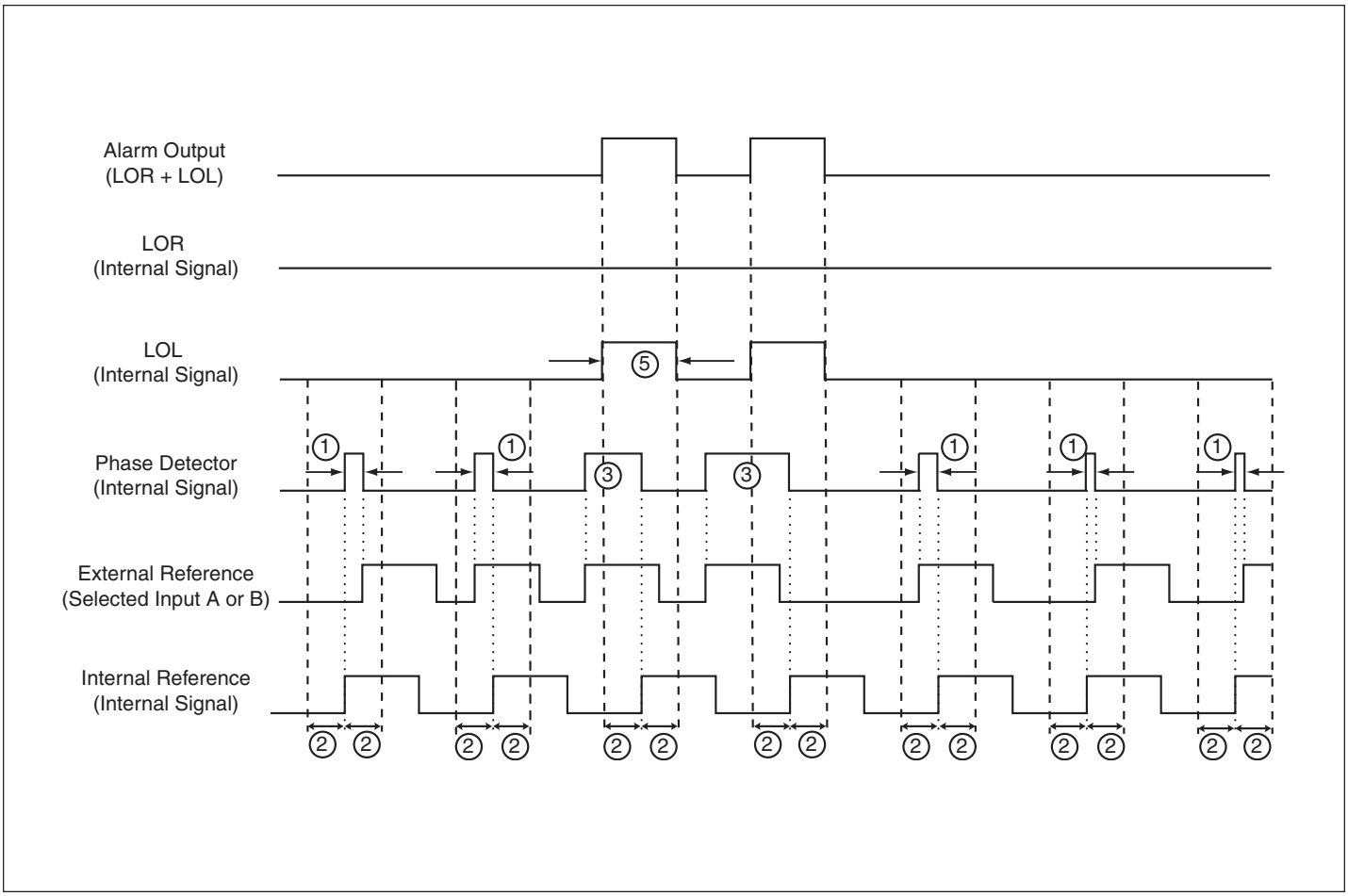
Loss of Lock Condition Alarm Timing

Figure 5



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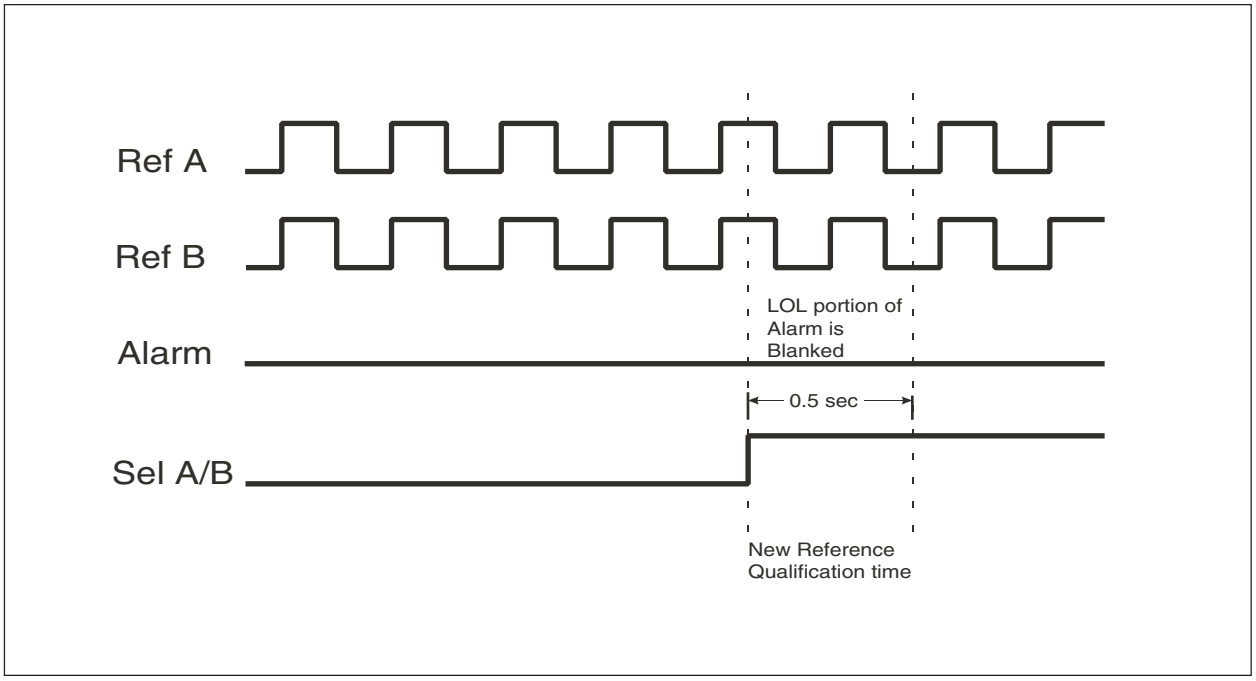
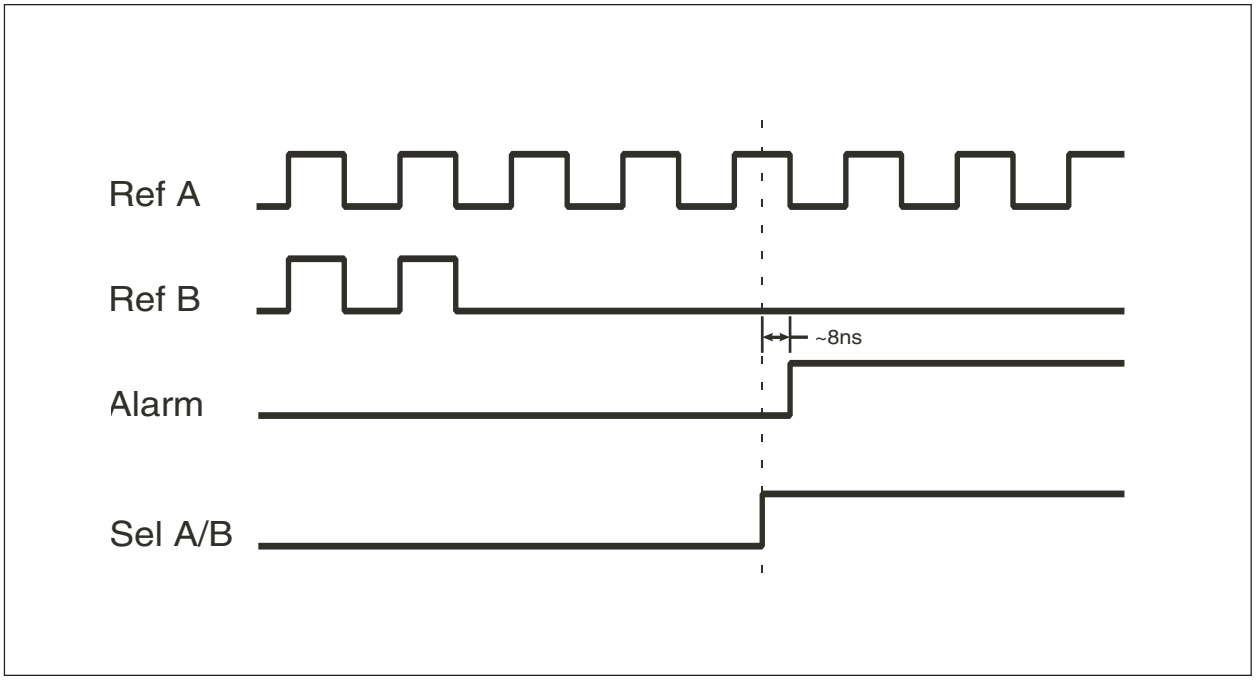
Switch from A to B when both are good signals

Figure 6



Switch from A to B when Reference B is lost

Figure 7



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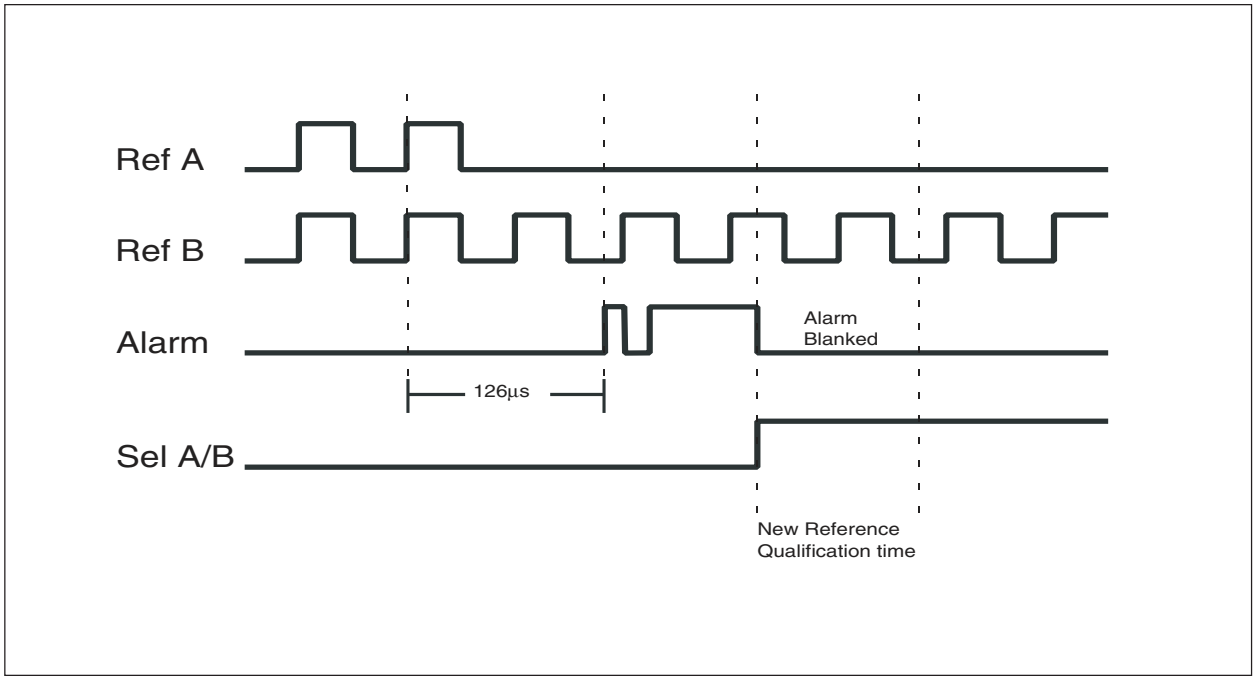
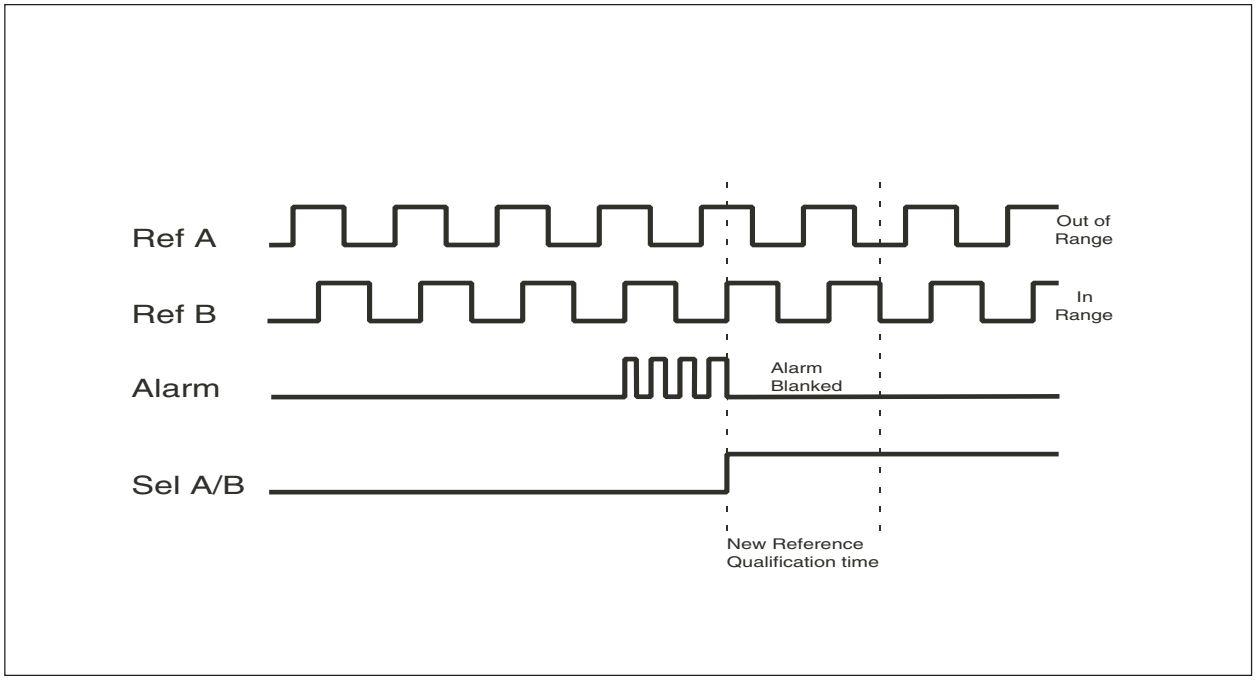
Switch from A to B after Reference A is lost

Figure 8



Switch from A to B when A is out of range

Figure 9



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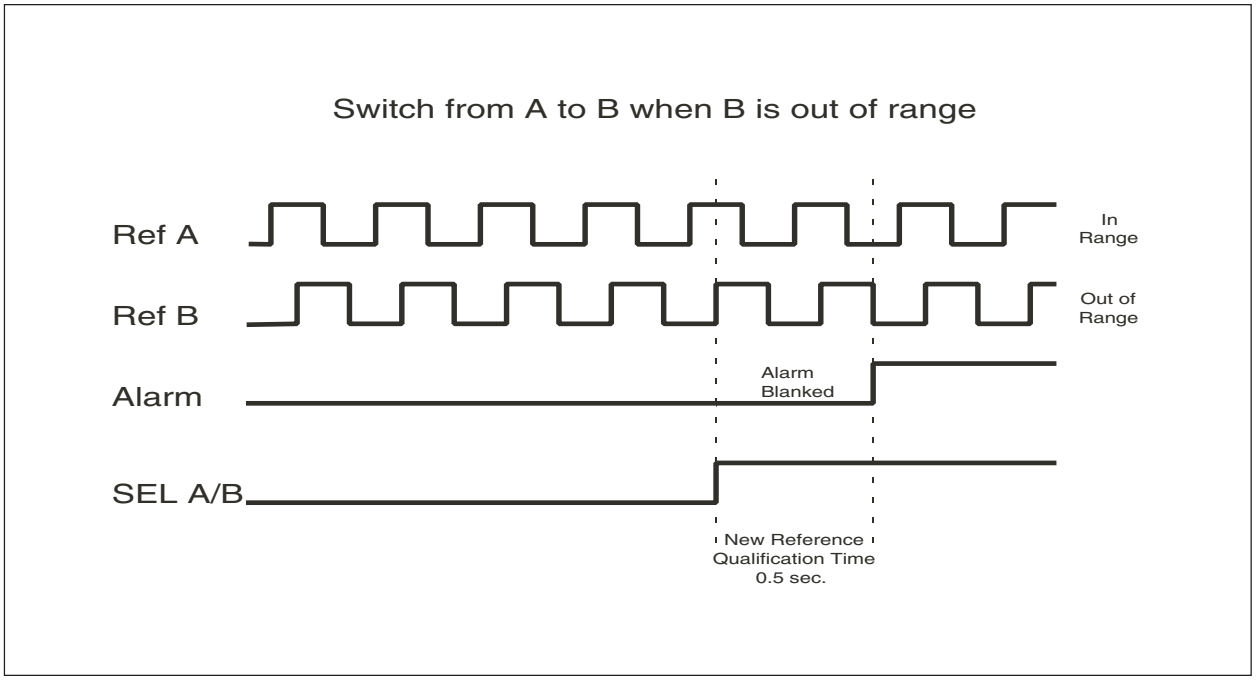
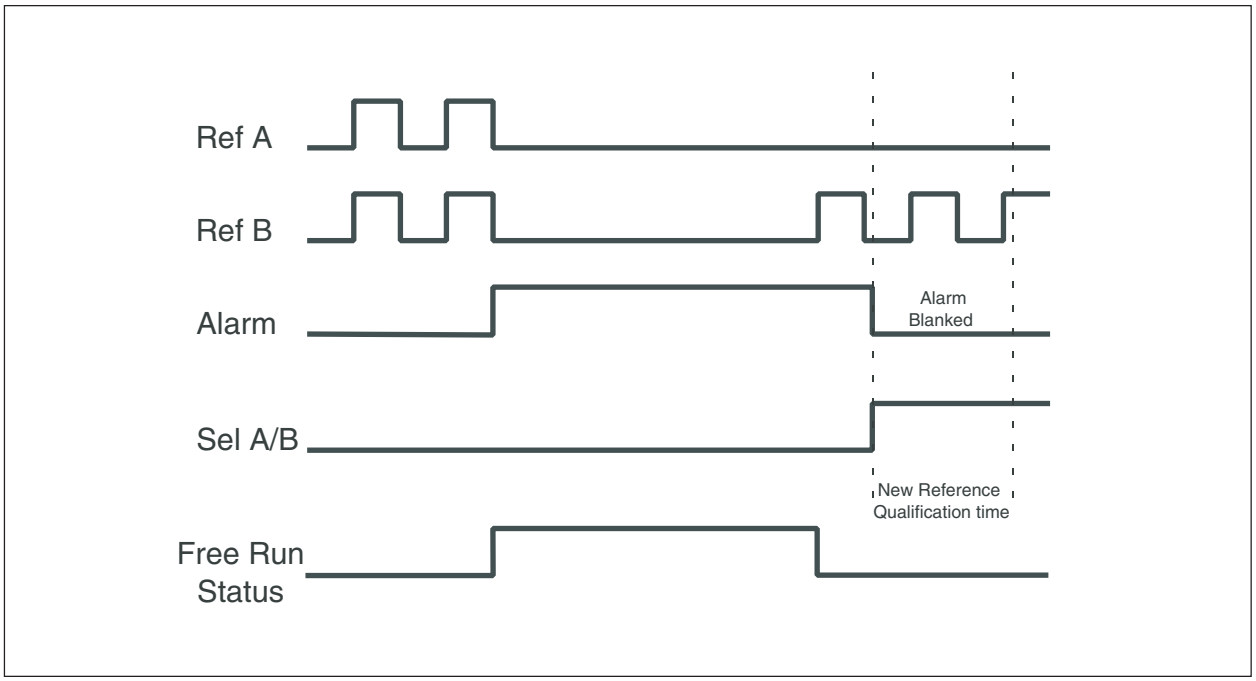
Switch from A to B when B is out of range

Figure 10



Switch from A to B when B is out of range

Figure 11



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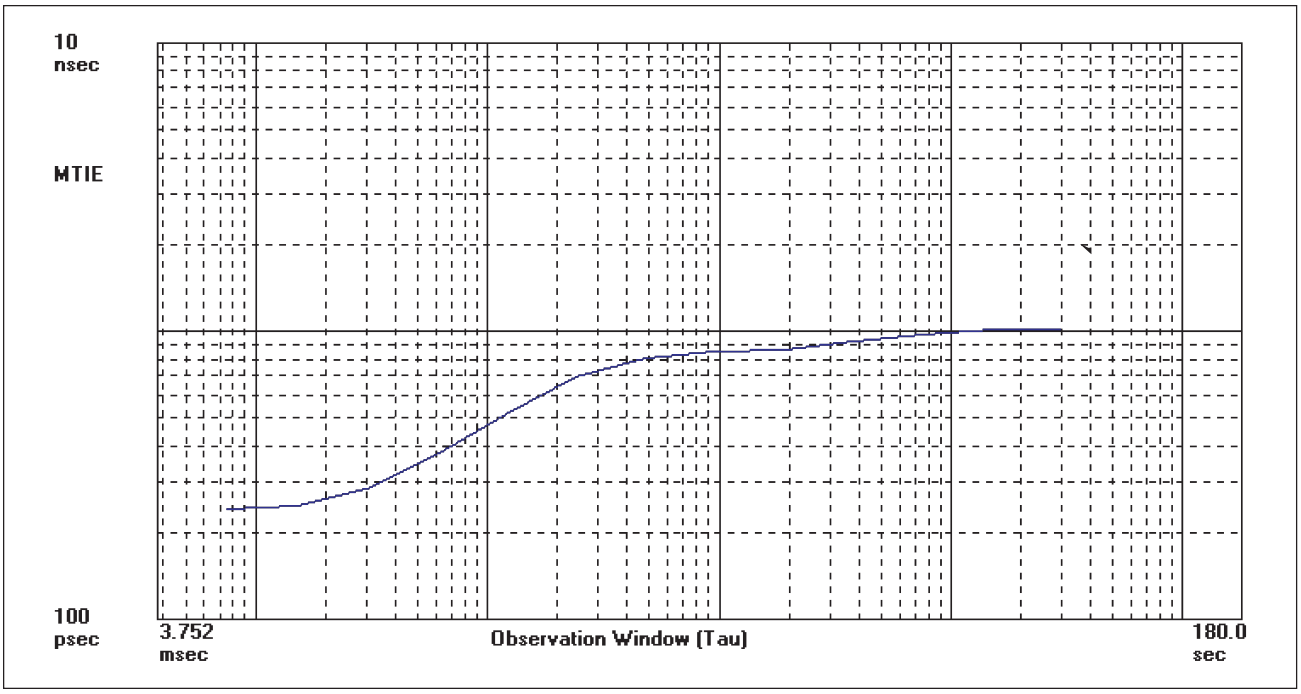
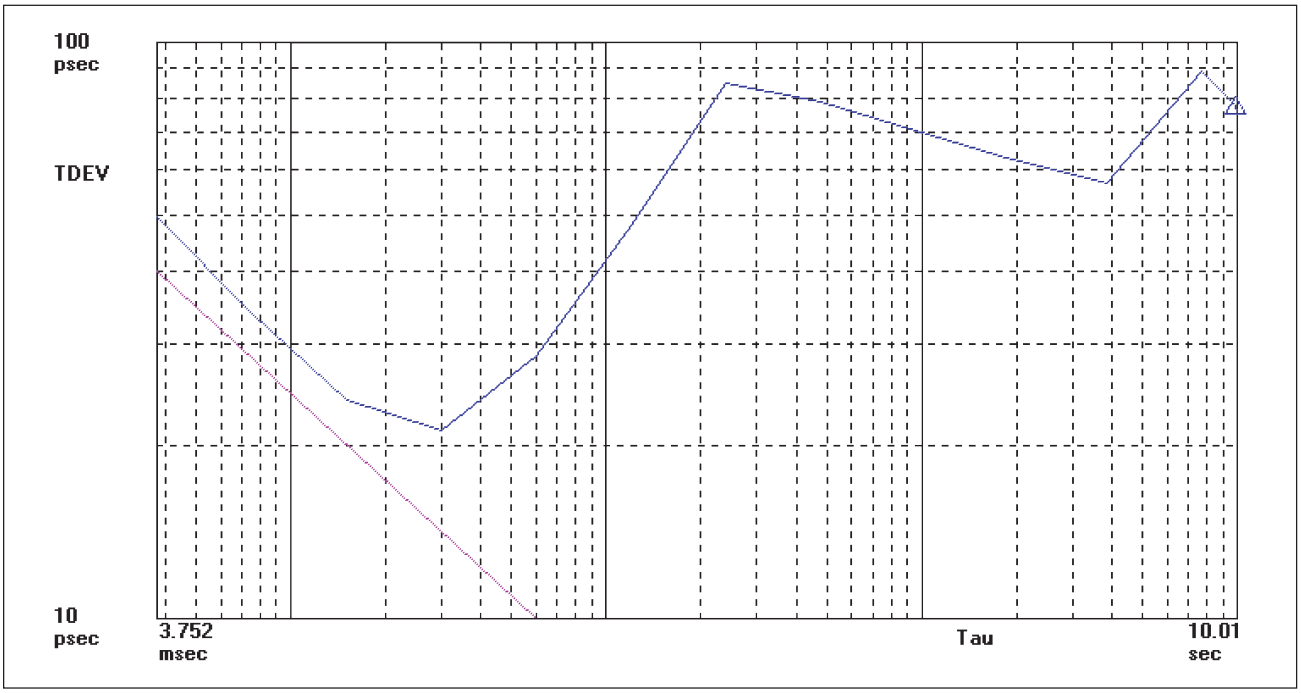
Typical MTIE Measurement

Figure 12



Typical TDEV Measurement

Figure 13



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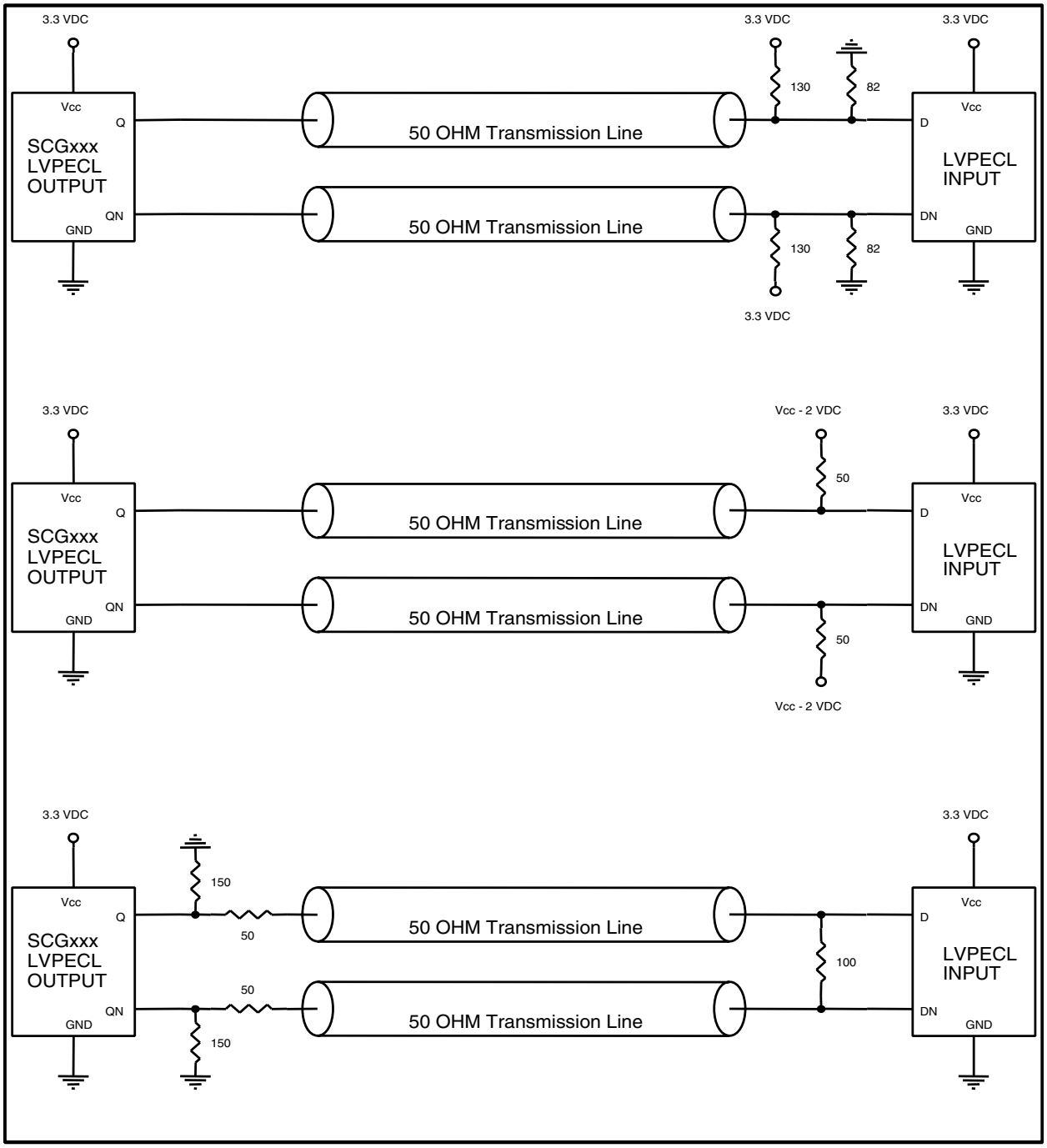
Recommended PECL Termination

Figure 14



If PECL outputs do not drive a long line (< 0.5”),
a single 150Ω termination resistor to ground may be used for each pin.

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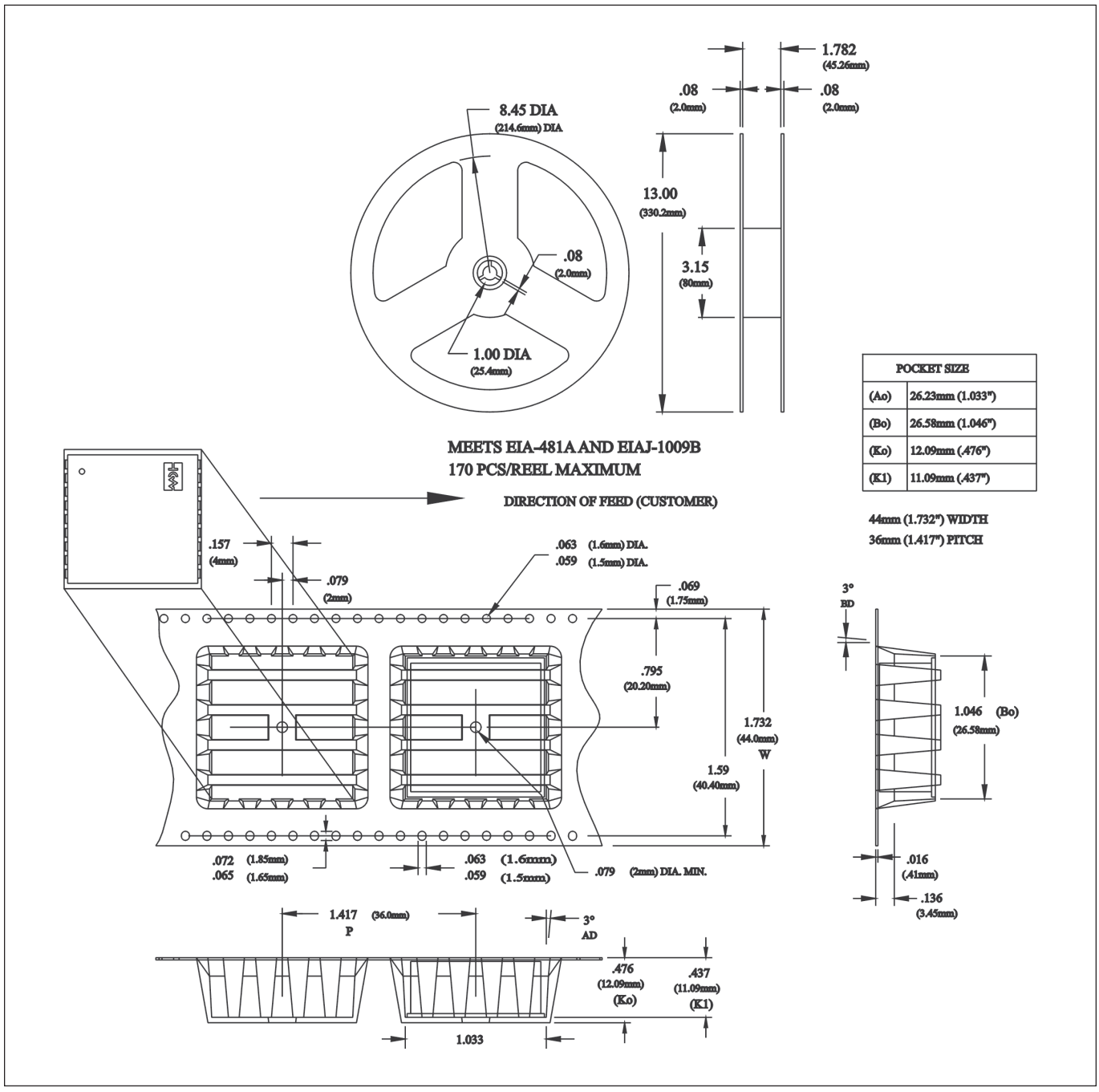
Tape and Reel Packaging

Figure 15



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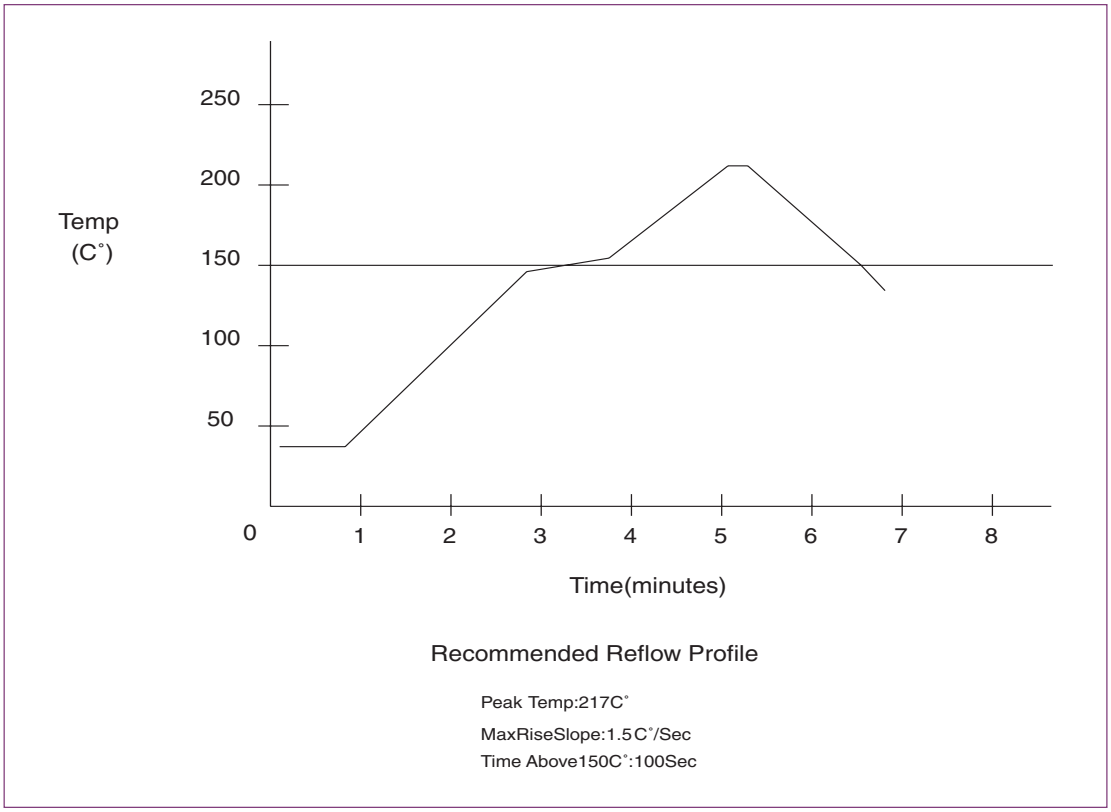
Solder Profile

Figure 16



Ordering Information

SCG{XXXX}-{FFF.FFF}{M}

XXXX equals a specific model (4505)
FFF.FFF equals the Oscillator Output frequency (077.76, 155.52)
M equals MHZ and is added to all part numbers

Example: To order an SCG4505 with an Oscillator Output of 155.52 MHz,
Order part number SCG4505-155.52M

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Revision	Revision Date	Note
P00	08/19/02	Preliminary informational release
P01	01/31/03	Added Acquisition timing to Table 2