SCG101
Synchronous Clock Generators

CONNOR WINFIELD

PLL

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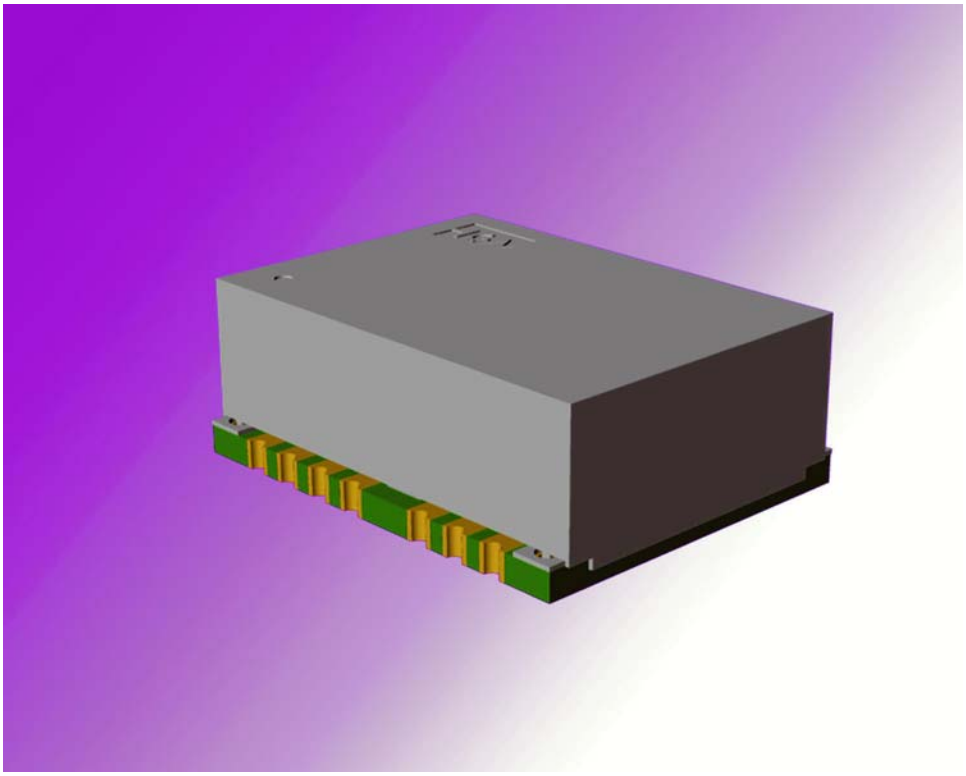

Application

The Connor-Winfield SCG101 is a 3.3V frequency translator based on a high frequency, crystal oscillator that is input duty cycle tolerant. The SCG101 accepts one input which may be controlled to accept up to four unique reference frequencies between 8 kHz to 170 MHz. The reference frequency selection is controlled by two input select pins.

The SCG101 locks to the input reference and provides a phase-locked HCMOS output at customer specified frequencies up to 125 MHz.

Features

- 3.3V High Precision PLL
- Tri-State Capability
- Input Reference Detector
- User Determined Input Reference
- Output Frequencies up to 125 MHz Available

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General Description

The SCG101 provides high precision phase lock loop frequency translation for the telecommunication applications. The SCG101 product generates a HCMOS output from an intrinsically low jitter, voltage controlled crystal oscillator.

SCG101 is well suited for use in line cards, service termination cards and similar functions to provide reliable reference, phase locked, synchronization for TDM, PDH, SONET and SDH network equipment . The SCG101 provides a jitter filtered, low phase gain (<0.2 dB), wander following output signal sychronized to a superior Stratum or peer input reference signal.

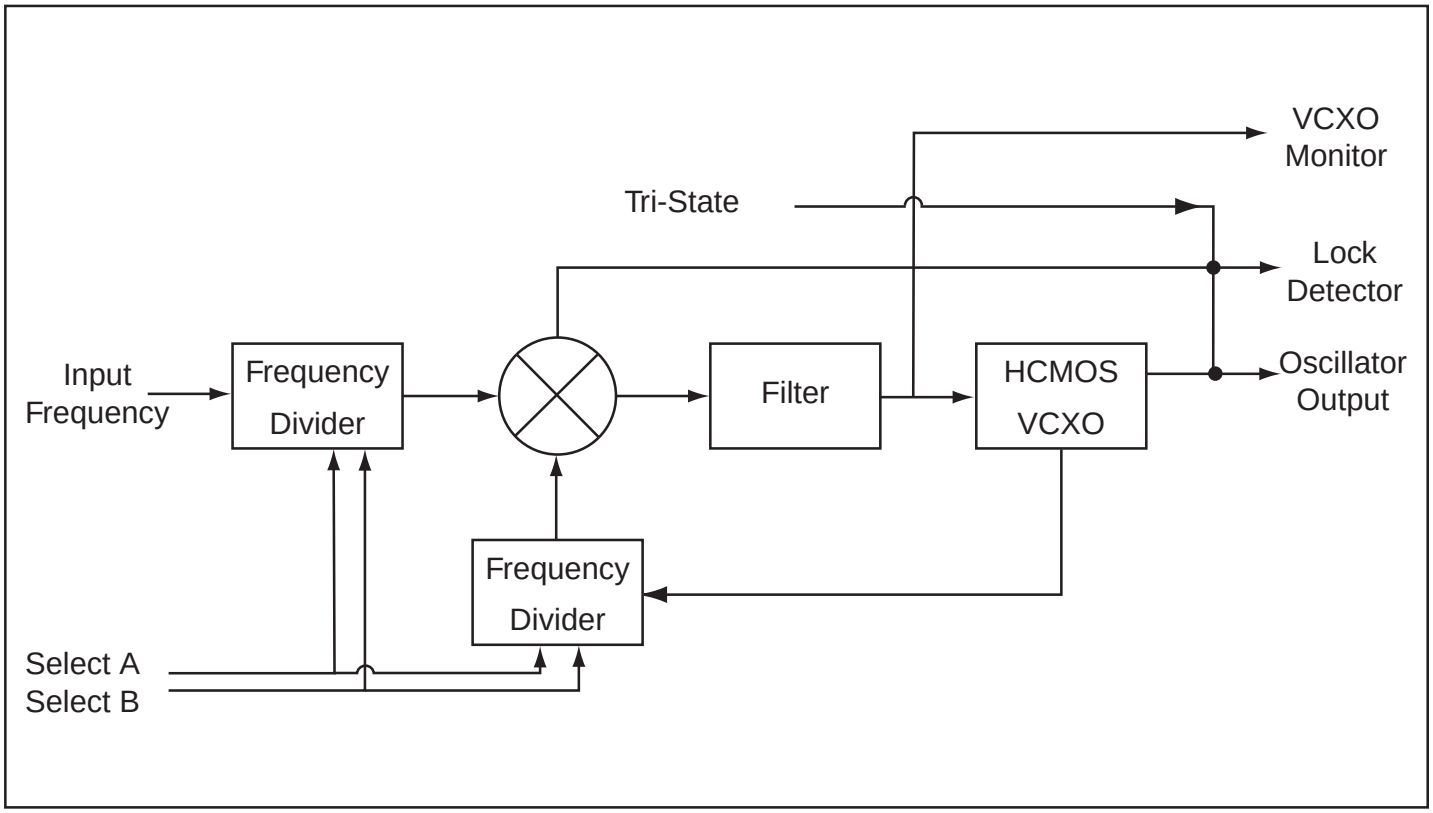
The SCG101 includes the following features: Tri-state and an alarm output for Loss-of-Reference, (LOR), Loss-of-Lock, (LOL). The HCMOS outputs may be put into the tri-state high impedance condition for external testing purposes by asserting a high signal to the Enable/Disable pin.

The SCG101 is a 3.3 Volt component that will typically draw 100mA. All models have a fast acquisition time of approximately 1 second and can be used in applications that require temperature rating of -40°C - 85° C. The SCG101 package typical dimensions are 1.025" x .80" x .375" (See fig. 2 for maximum dimensions). Parts are assembled using high temperature solder to withstand surface mount reflow process.

The SCG101 locks to any one of four input reference frequencies. The unit may have up to four different frequencies as long as all frequencies are evenly divisible by 8 kHz. The output may be any single frequency up to 125 MHz.

Functional Block Diagram

Figure 1



Absolute Maximum Rating

Table 1

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
Vcc	Power Supply Voltage	-0.5		4	Volts	
V1	Input Voltage	-0.5		5.5	Volts	
Ts	Storage Temperature	-65		150	°C	

Specifications

Table 2

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
Vcc	Supply Voltage	3.3 - 5%	3.3	3.3 + 5%	Volts	
I_{CC}	Supply Current		100		mA	
Input Frequencies(HCMOS/LVHCMOS)		8 k		170 M	Hz	
Output Frequencies(LVPECL)		16.384		125	MHz	
DC	Positive Duty Cycle	45		55	%	
T_R/T_F	Rise/Fall Time (10%-90%)		3	5	ns	
APR	Input Frequency Tracking	±32			ppm	
BW	Bandwidth			15	Hz	
J_{GEN}	Jitter Generation RMS (12 kHz - 20 MHz)		0.5	1	ps	
J_{TRAN}	Jitter Transfer			0		1
J_{TOL}	Jitter Tolerance					
	8 kHz References	≥31.35			µs	2
	19.44 MHz References	>1			µs	2
Φ	Phase Gain			0.2 dB @~0.1 Hz		
T_{OP}	Operating Temperature	-40		85	°C	

NOTES: 1.0: All jitter is attenuated (≥10 Hz)
` 2.0: Jitter transfer refers to the magnitude of input jitter tolerance that results in an alarm.

Pin Description

Table 3

Pin #	Connection	Description
1	Reference Input	Reference Input
2	GND	Ground
3	Lock Detector	Logic “1” indicates that the unit is locked to the input reference Logic “0” indicates that the unit is has lost its reference Pulsing indicates that the unit is no longer locked to a reference.
4	VCXO Monitor	Control voltage level for the PECL oscillator
5	----	Missing
6	NC	No connection
7	GND	Ground
8	Tri-State	Logic “1” = output in high impedance Logic “0” = output normal (or No Connect)
9	Oscillator Output	HCMOS oscillator output
10	GND	Ground
11	NC	No connection
12	Input Freq. Select A	Control pin A used to select input frequency. Input is pulled to GND.
13	Input Freq. Select B	Control pin B used to select input frequency. Input is pulled to GND.
14	NC	No connection
15	GND	Ground
16	V_{CC}	Power supply voltage (3.3 Vdc ± 5%)

Reference Frequency Selection Table

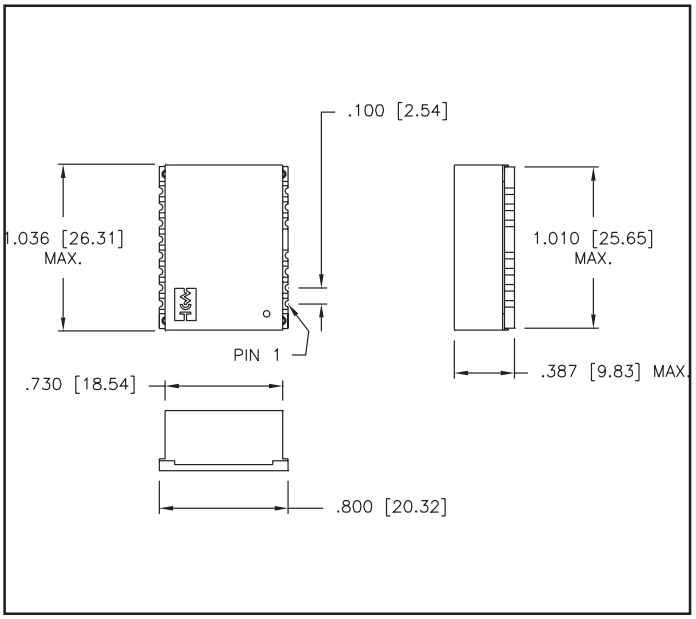
Table 4

Input Frequency*	SelA	SelB
f_1	0	0
f_2	0	1
f_3	1	0
f_4	1	1

* Input frequencies are determined by the customer. See pg.6 for more detailed ordering information.

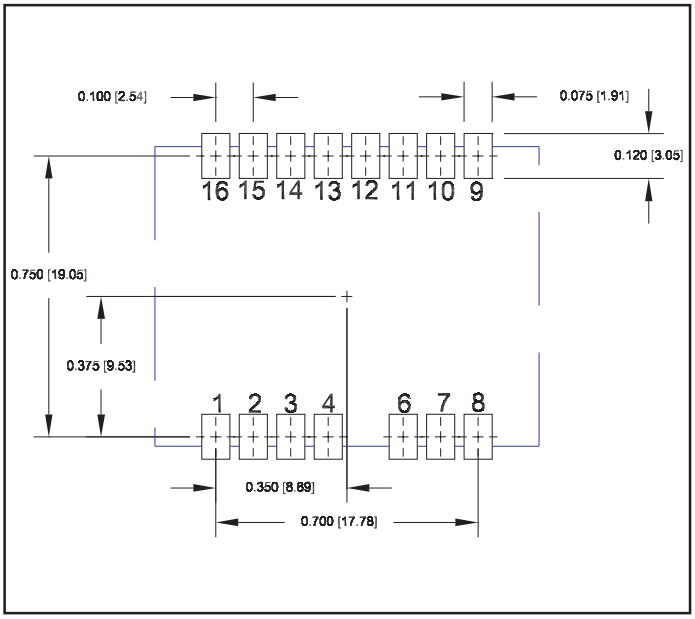
Package Dimensions

Figure 2



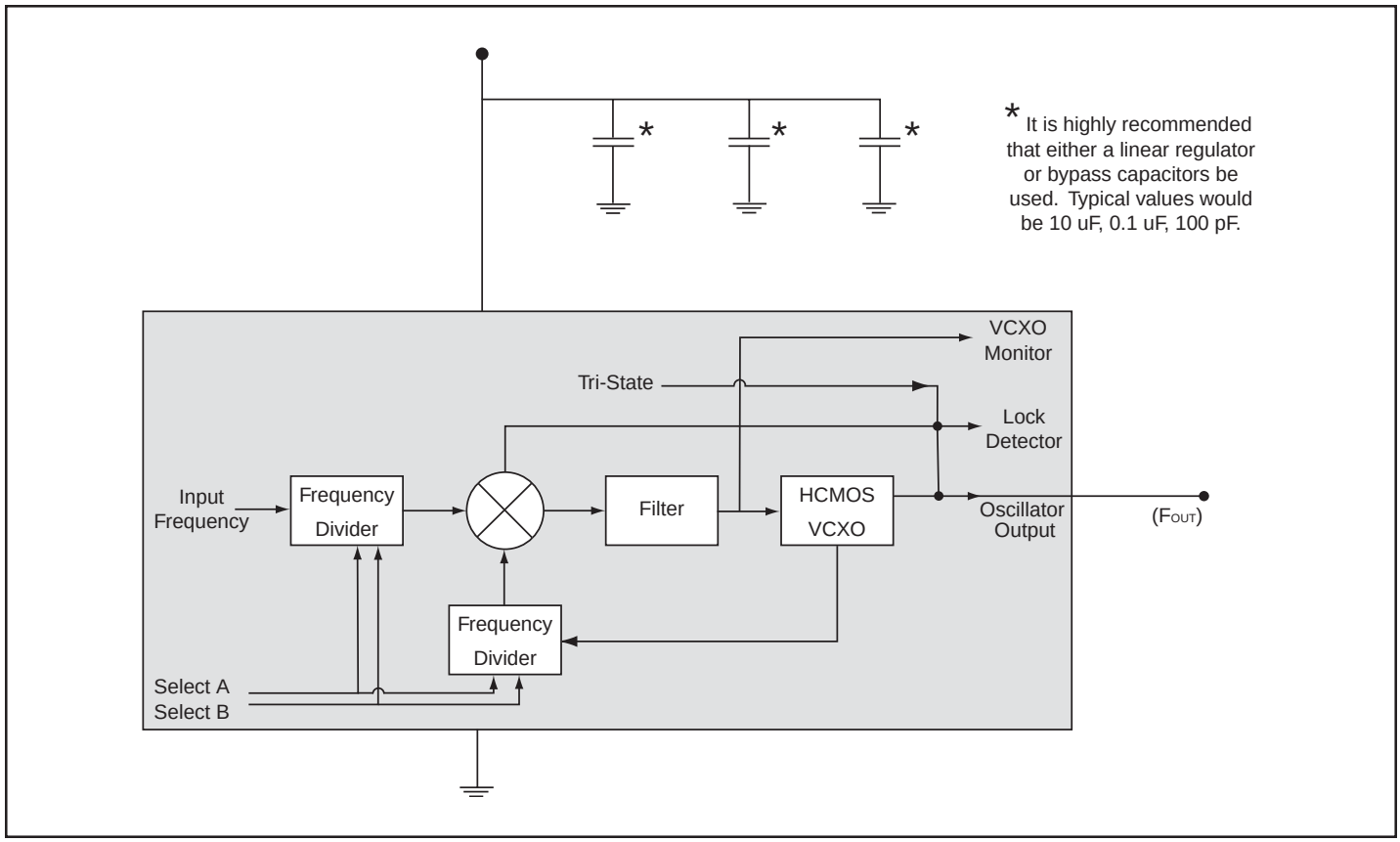
Recommended Footprint Dimensions

Figure 3



Power Supply Filtering Recommendations

Figure 4



Ordering Information

8 kHz	C	16.384 MHz	N		
16 kHz	D	19.44 MHz	P	77.76 MHz	2
64 kHz	E	20.48 MHz	R	139.264 MHz	5
1.024 MHz	F	38.88 MHz	X	155.52 MHz (Input Only)	6
1.544 MHz	H	44.736 MHz	Y	166.6286 MHz (Input Only)	7
2.048 MHz	J	64.44 MHz	1	Special SCD	S

SCG-101- D F F - A 1 P 6

Supply Voltage
D = 3.3 V_{DC} ± 5%

Output Type
A = HCMOS

Temperature Range
C = 0°C to 70°C
F = -40°C to 85°C

Output Frequency (2 to 7)
See chart above.
Contact a sales representative for the availabilty of custom frequencies.

Input Frequency (C to 7)
See chart above.
If more than one frequency is desired, enter **S** and list all desired frequencies.
Contact a sales representative for the availabilty of custom frequencies.

Number of Input Frequencies
1 = 1 Input Frequency
2 = 2 Input Frequencies
3 = 3 Input Frequencies
4 = 4 Input Frequencies

Input Logic
A = CMOS

Sample Part Number Examples:
SCG-101- DFF-A1C2
SCG-101- DFF-A4S2, S = 8 kHz, 16.384 MHz, 19.44 MHz, 38.88 MHz

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