SCG2230G Synchronous Clock Generator

PLL

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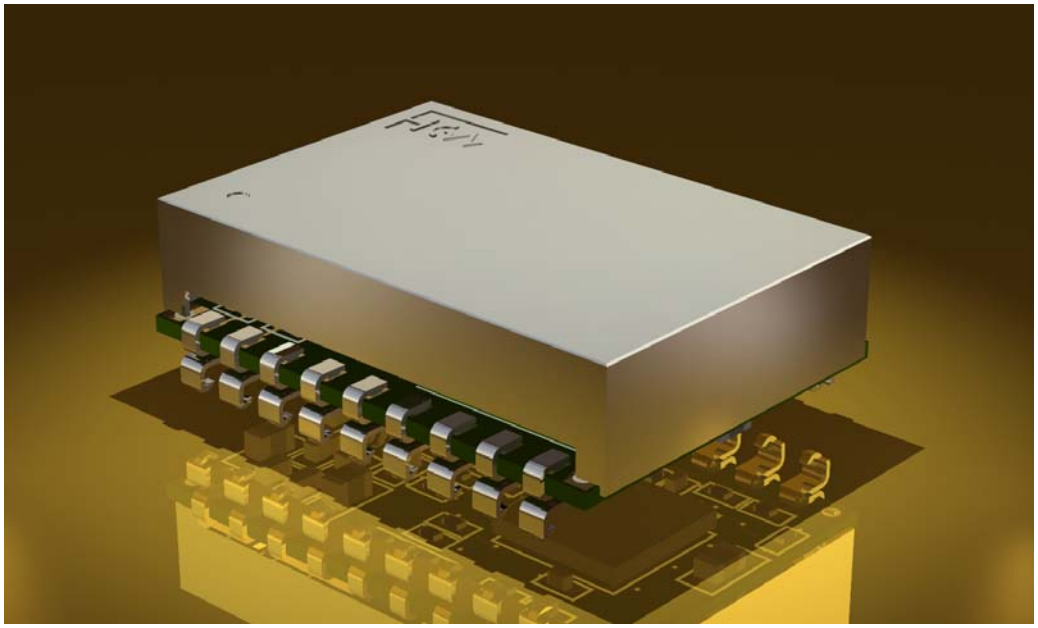

Application

The Connor-Winfield SCG2230G provides high precision phase lock loop frequency translation for the telecommunication applications.

SCG2230G is well suited for use in line cards, service termination cards and similar functions to provide reliable reference, phase locked, synchronization and low phase gain for TDM, PDH, SONET and SDH network equipment. The SCG2230G provides a jitter filtered, wander following output signal synchronized to a superior Stratum or peer input reference signal. This product is compliant with all required ROHS specifications.

Features

- **3.3V High Precision PLL**
- **1 Complimentary LVPECL Output**
- **2 CMOS Outputs**
- **Selectable Output Frequencies**
- **Footprint Compatible with SCG2000 Series**
- **Active Alarms**
- **Guaranteed Free Run ±20ppm**
- **1 Sec. Acquisition Time**
- **ROHS compliant**

RoHS COMPLIANT

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General Description

The SCG2230G like the SCG2000 Series, provides high precision phase lock loop frequency translation for the telecommunication applications. The SCG2230G generates an LVPECL differntial output and two LVCMOS outputs from an intrinsically low jitter, voltage controlled crystal oscillator. The SCG2230G also provides a jitter attenuated, internal reference that is connected to a Reference Output pin. Further, SCG2230G allows user selection of internal dividers for output frequency selection.

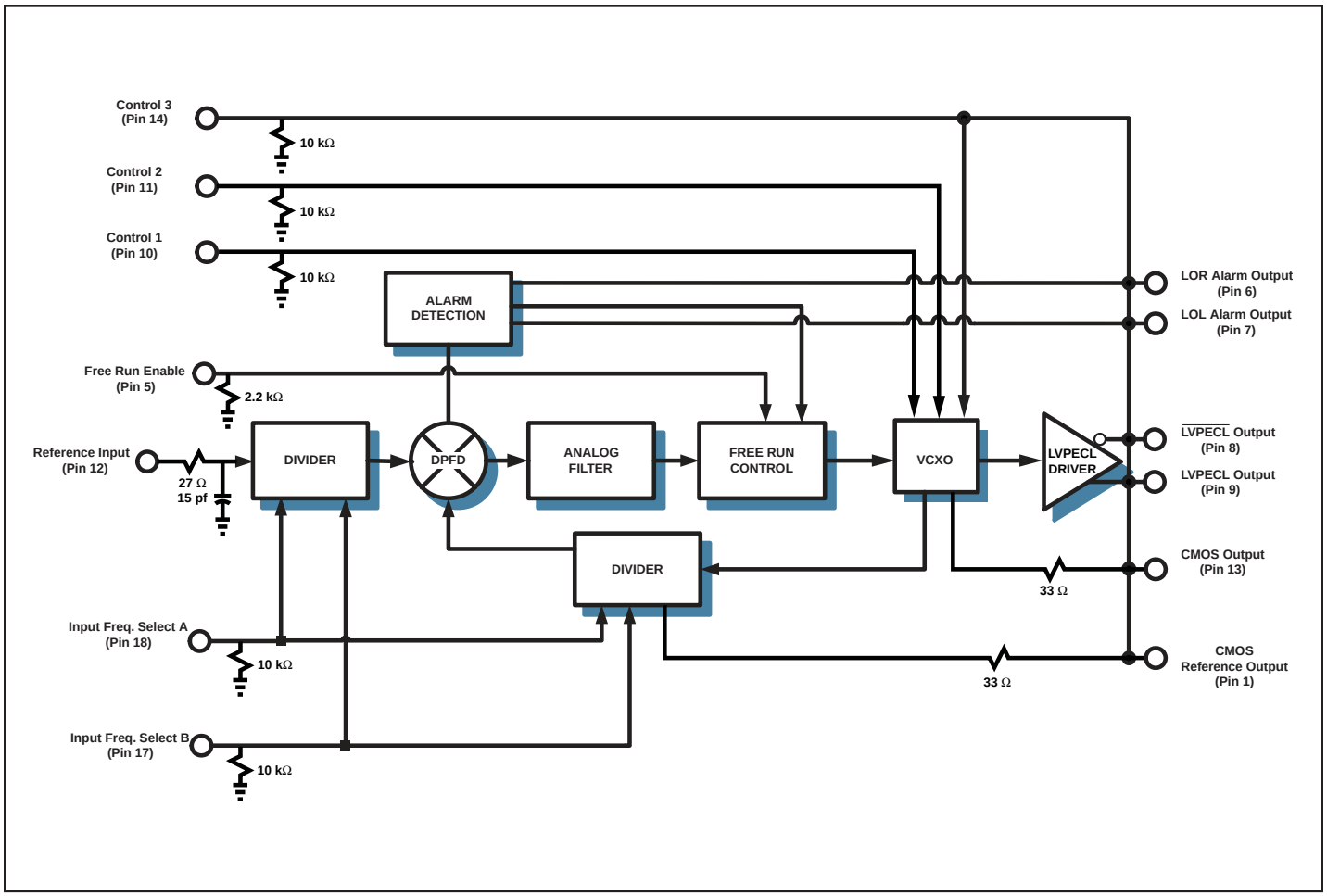
SCG2230G is well suited for use in line cards, service termination cards and similar functions to provide reliable reference, phase locked, synchronization for TDM, PDH, SONET and SDH network equipment . The SCG2230G provides a low phase gain (<0.2dB), jitter filtered, wander following output signal synchronized to a superior Stratum or peer input reference signal.

The SCG2230G include the following features: Selectable output frequencies, Free Run, Tri-state, alarm outputs for Loss-of-Reference, (LOR), Loss-of-Lock, (LOL) and 3 output frequencies (1LVPECL, 2 LVCMOS). During the LOR alarm, the SCG2230G will also enter a Free Run state which will guarantee a 20 ppm accurate output. Additionally the Free Run mode may be entered manually by asserting a high signal to the Free Run Enable pin.

The SCG2230G are 3.3 Volt components that typically draw less than 200 mA. The SCG2230G has an acquisition time of approximately 1.0 second and can be used in applications that require temperature rating of 0° - 70° C. The SCG2230G maximum package dimensions are .78" x 1.03" x .35" on a six layer FR4 board with surface mount pins. The SCG2230G footprint is compatible with the SCG2000 Series footprint with use of a slightly longer footprint to allow use of either product for maximum efficiency. Parts are assembled using high temperature solder to withstand surface mount reflow process and is ROHS compliant.

Functional Block Diagram

Figure 1



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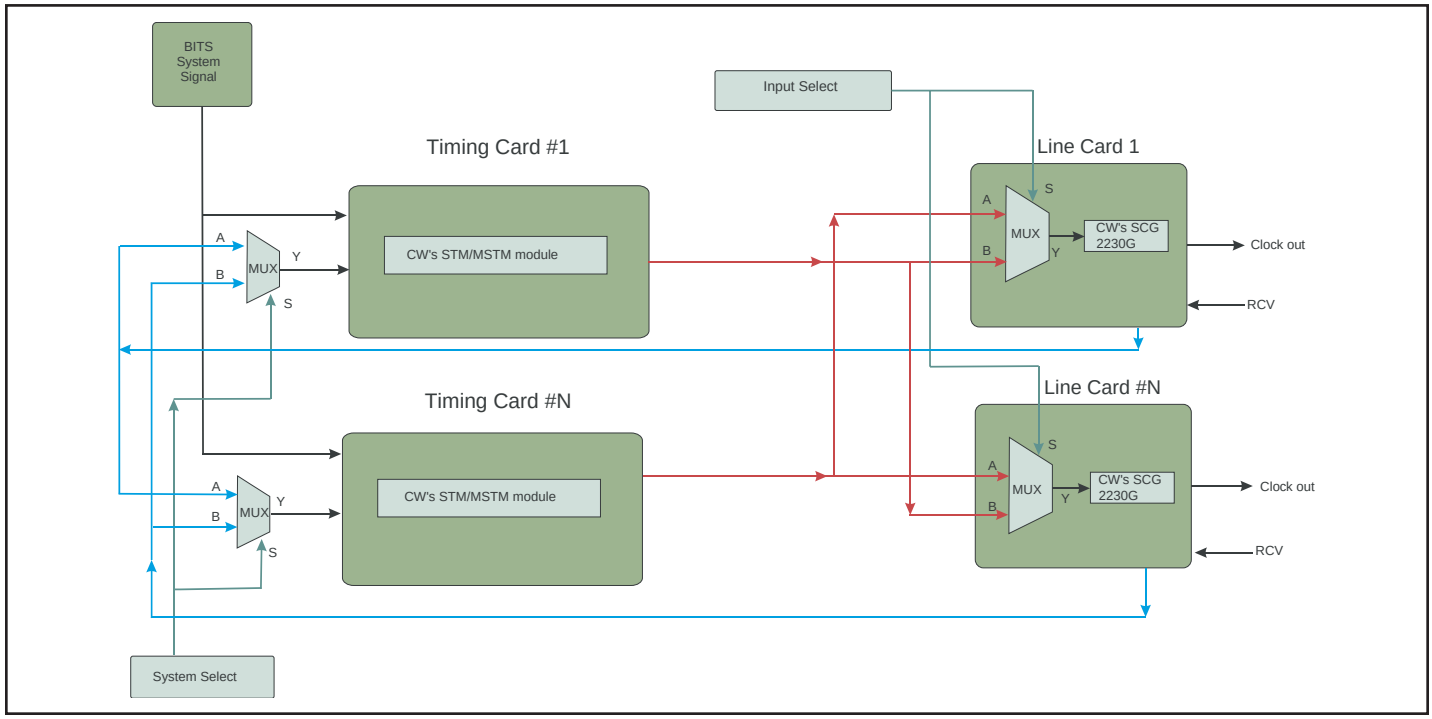
Pin Description

Table 1

Pin #	Connection	Description
1	Reference Output	Reference Output frequency is equal to Reference Input frequency
2	TCK	JTAG pin that is used only by Connor-Winfield for programming. Do not connect
3	TMS	JTAG pin that is used only by Connor-Winfield for programming. Do not connect
4	Ground	Ground
5	Free Run Enable/TDI	Free Run enable pin. 1 = Free Run at selected output frequency ±20ppm. Default = 0. See Table 8
6	Loss of Reference (LOR)	Alarm indicator. 1 = The reference has been lost.
7	Loss of Lock (LOL)	Alarm indicator. 1 = Phase lock has been lost
8	$\overline{\text{LVPECL}}$	Negative Differential LVPECL output
9	LVPECL	Positive Differential LVPECL output
10	Control 1	Output frequency control pin #1. Default = 0. See Table 7
11	Control 2	Output frequency control pin #2. Default = 0. See Table 7
12	Reference Input	Input reference frequency.
13	CMOS Output	High frequency CMOS output.
14	Control 3	Output frequency control pin #3. Default = 0. See Table 7
15	Vcc	3.3V Supply Voltage.
16	TDO	JTAG pin that is used only by Connor-Winfield for programming. Do not connect
17	Input Freq. Select B	Control pin B used to select input frequency. Default = 0. See Table 9
18	Input Freq. Select A	Control pin A used to select input frequency. Default = 0. See Table 9

Typical Application

Figure 2



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Absolute Maximum Rating

Table 2

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
Vcc	Power Supply Voltage	-0.3		3.8	Volts	
V1	Input Voltage	-0.5		5.5	Volts	
Ts	Storage Temperature	-40		85	deg. C	

Specifications

Table 3

Parameter	Specifications	Notes
Input Reference Frequencies	8, 16, 32 & 64 kHz (Option G) or 19.44 MHz (Option F)	See Table 9
Output Reference Frequencies	Equal to selected input reference frequency	1.0
LVPECL Output Freq (Max)	170 MHz (VCXO Freq. = f_{Osc})	
LVCMOS Output	$f_{Osc}/2$ (See Table 7)	
Voltage	3.3V ±5%	2.0
Current	200 mA Maximum	
Temperature Range	0 to 70°C	
Input Jitter Tolerance *(Input Jitter Frequencies ≥ 10 Hz)*	≥31.25us (Option G) ≥1 us (Option F)	
Jitter Bandwidth	<15 Hz	
Acquisition Time	Approx 1.0 second	3.0
Capture/Pull-in Range	±25 ppm Minimum	
Alarms	LOR, LOL Status on seperate outputs	
Free Run Accuracy	±20 ppm	
Package	Fr4 SM 0.78" x 1.03" x 0.35" (maximum)	
TDEV	60 ps Typical	
MTIE	750 ps Typical	
Reference Output/Oscillator Output Offset	≤ 8 ns	
Static Offset (@25°C)	± 35 ns Maximum	4.0
Dynamic Offset (25°- 70°C)	± 15 ns Maximum	5.0
Dynamic Offset (0°- 70°C)	± 20 ns Maximum	5.0

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Output Jitter Specifications

Table 4

	Jitter BW 10 Hz - 20 MHz		SONET Jitter BW 12 KHz - 20 MHz	
Frequency (MHz)	pS (RMS)	mUI	pS (RMS)	m UI
77.76 (CMOS Output)	10 Typ.	0.778 Typ.	3 Max.	0.233 Max.
155.55 (LVPECL Output)	10 Typ.	1.55 Typ.	1 Max.	0.155 Max.
163.84 (LVPECL Output)	10 Typ.	1.64 Typ.	1 Max.	0.164 Max.
166.6285 (LVPECL Output)	15 Typ.	2.50 Typ.	1 Max.	0.167 Max.

Input And Output Characteristics

Table 5

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
CMOS Input Characteristics						
V_{IH}	High Level Input Voltage	2	-	5.5	V	
V_{IL}	Low Level Input Voltage	0	-	0.8	V	
T_{IO}	I/O to Output Valid	-	-	10	nS	
T_{IR}	Input Reference Signal Pulse Width	30	-		nS	
LVCMOS Output Characteristics						
C_O	Output Capacitance	-	-	10	pF	
V_{OH}	High Level Output Voltage I_{oH} = -6mA High Level Output Voltage I_{oH} = -100uA	2.2 2.9	- -		Vdc Vdc	
V_{OL}	Low Level Output Voltage I_{oL} = 6mA Low Level Output Voltage I_{oL} = 100uA	- -	- -	0.7 0.2	Vdc Vdc	
DC	Output Duty Cycle at 50% level	45	50	55	%	
T_{RF}	Rise and Fall Time (20% - 80%)	-	-	2	ns	
LVPECL Output Characteristics						
L	Load	-	-	50	Ω	6.0
V_{OH}	Output Voltage High	V_{DD}-1.18	-	V_{DD}-0.81	V_{dc}	6.0
V_{OL}	Output Voltage Low	V_{DD}-1.98	-	V_{DD}-1.55	V_{dc}	6.0
DC	Output Duty Cycle at 50% level	45	50	55	%	
T_{RF}	Rise and Fall Time (20% - 80%)	-	-	350	ps	

NOTES:
1.0: Units with option D selected as an output frequency, buffer the reference input and supply it as the reference output without any jitter attenuation.
2.0: Requires external regulation
3.0: Frequency Lock from a 20 ppm offset in reference frequency
4.0: Offset between Reference Input and the Reference Output at room temperature.
5.0: Offset between Reference Input and the Reference Output over the entire specified temperature range.
6.0: 50Ω termination into Vcc-2V or Thevinin equivalent.

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Alarm Status

Table 6

LOL Output	LOR Output	Alarm Output
0	0	No alarm
1	0	Loss-of-Lock
X	1	Loss-of-Reference

Output Frequency Selection

Table 7

Control 3 (Pin #14)	Control 2 (Pin #11)	Control 1 (Pin #10)	LVPECL Output Frequency	CMOS Output Frequency
0	0	0	f_{Osc}	$f_{Osc}/2$
0	0	1	f_{Osc}	f_{Osc}*
0	1	0	f_{Osc}	$f_{Osc}/4$
0	1	1	$f_{Osc}/2$	$f_{Osc}/2$
1	0	0	Tri-State	Tri-State
1	0	1	$f_{Osc}/2$	$f_{Osc}/4$
1	1	0	$f_{Osc}/4$	$f_{Osc}/4$
1	1	1	$f_{Osc}/4$	$f_{Osc}/8$

* Not supported on standard product. Contact a Connor-Winfield Corp. representative if this mode of operation is required.

Free Run Control

Table 8

Free Run (Pin #5)	Operation
0	Locked to reference selected
1	Free Run at the selected output frequency

Input Reference Selection* (Option G)

Table 9

Input Sel A (Pin #18)	Input Sel B (Pin #17)	Reference Frequency (Pin #12)	Notes
0	0	8 kHz (default)	
1	0	16 kHz	
0	1	32 kHz	Not applicable when CMOS output equals 19.44MHz
1	1	64 kHz	Not applicable when CMOS output equals 19.44MHz or 38.88 MHz

*Does not apply to units that use 19.44 MHz as input reference.

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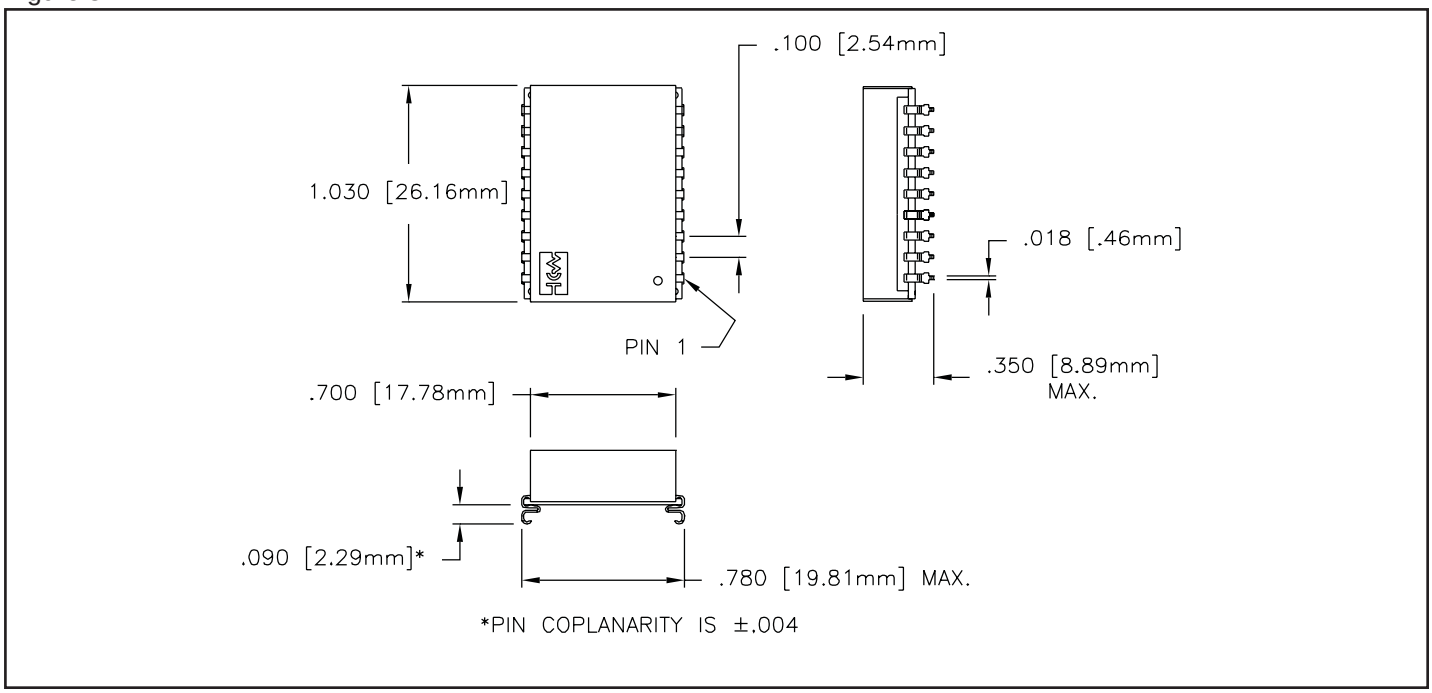
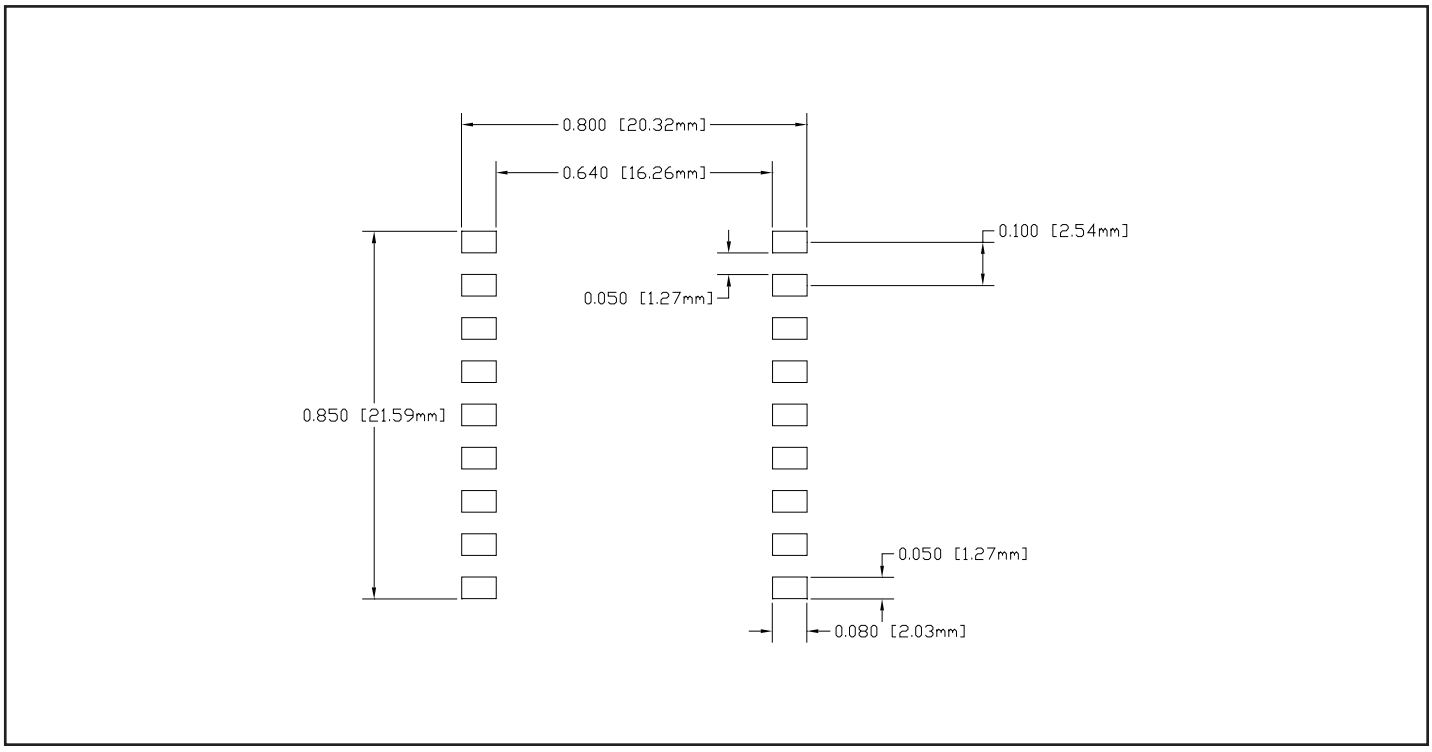
Maximum Package Dimensions

Figure 3



Recommended Footprint Dimensions

Figure 4



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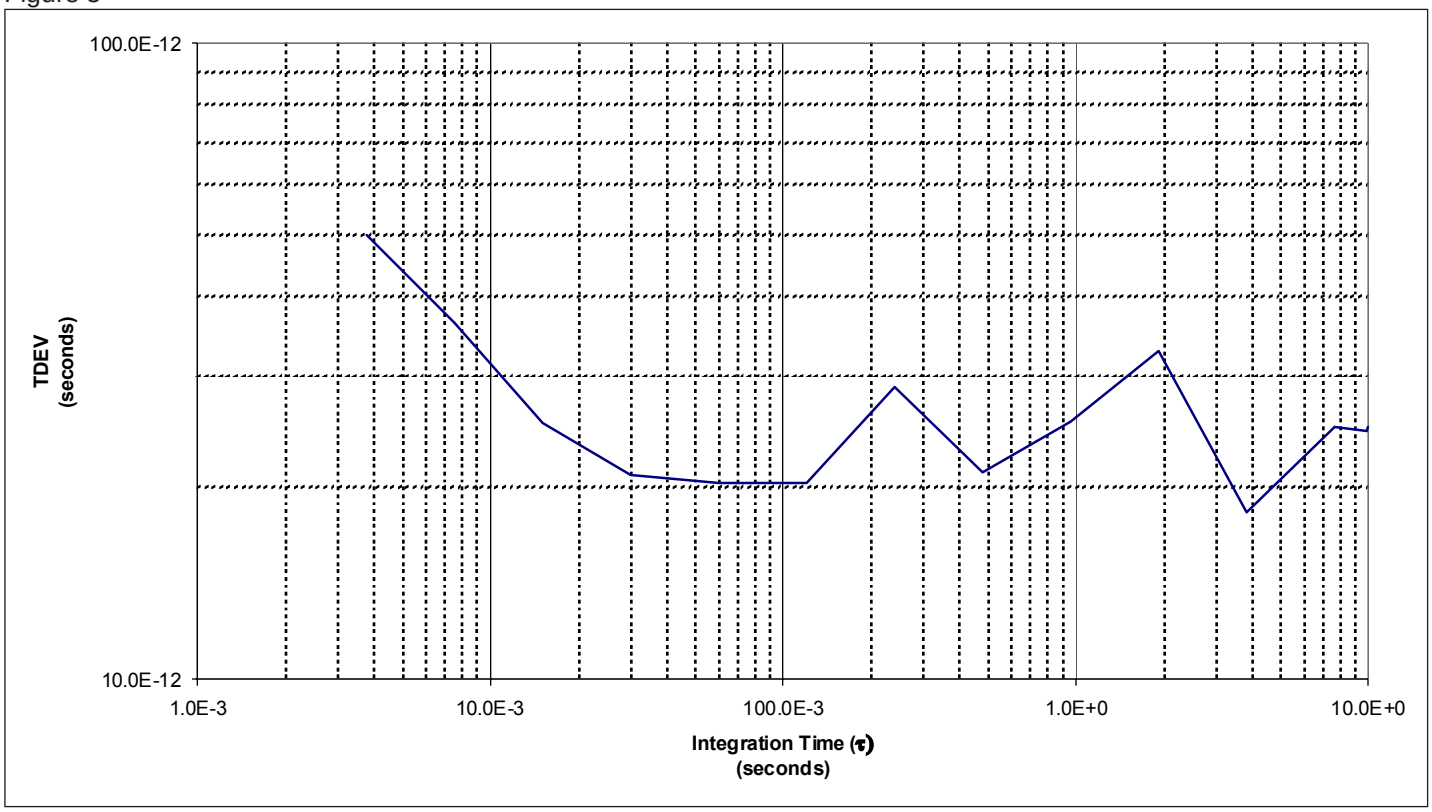
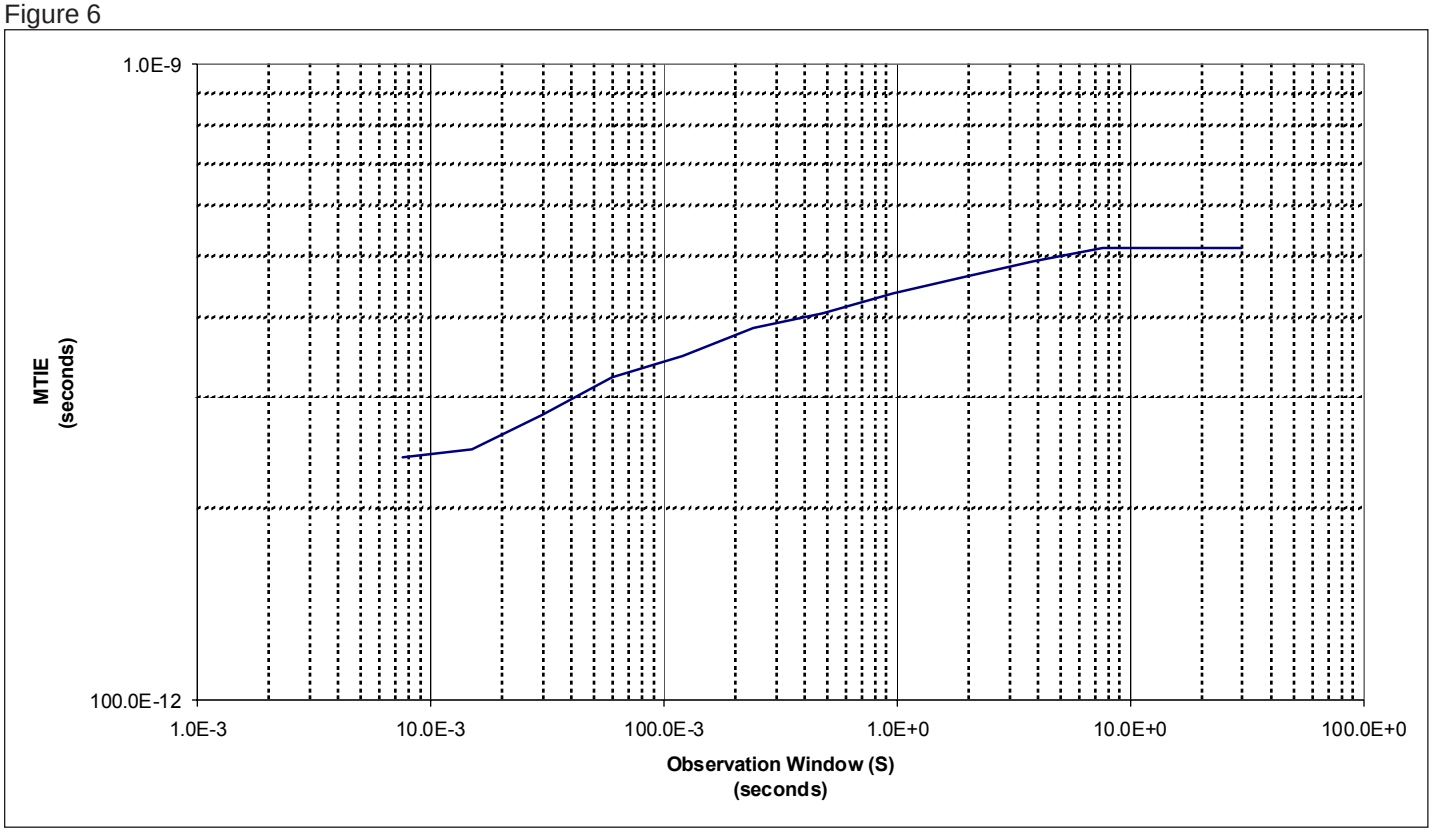
Typical TDEV

Figure 5



Typical MTIE

Figure 6



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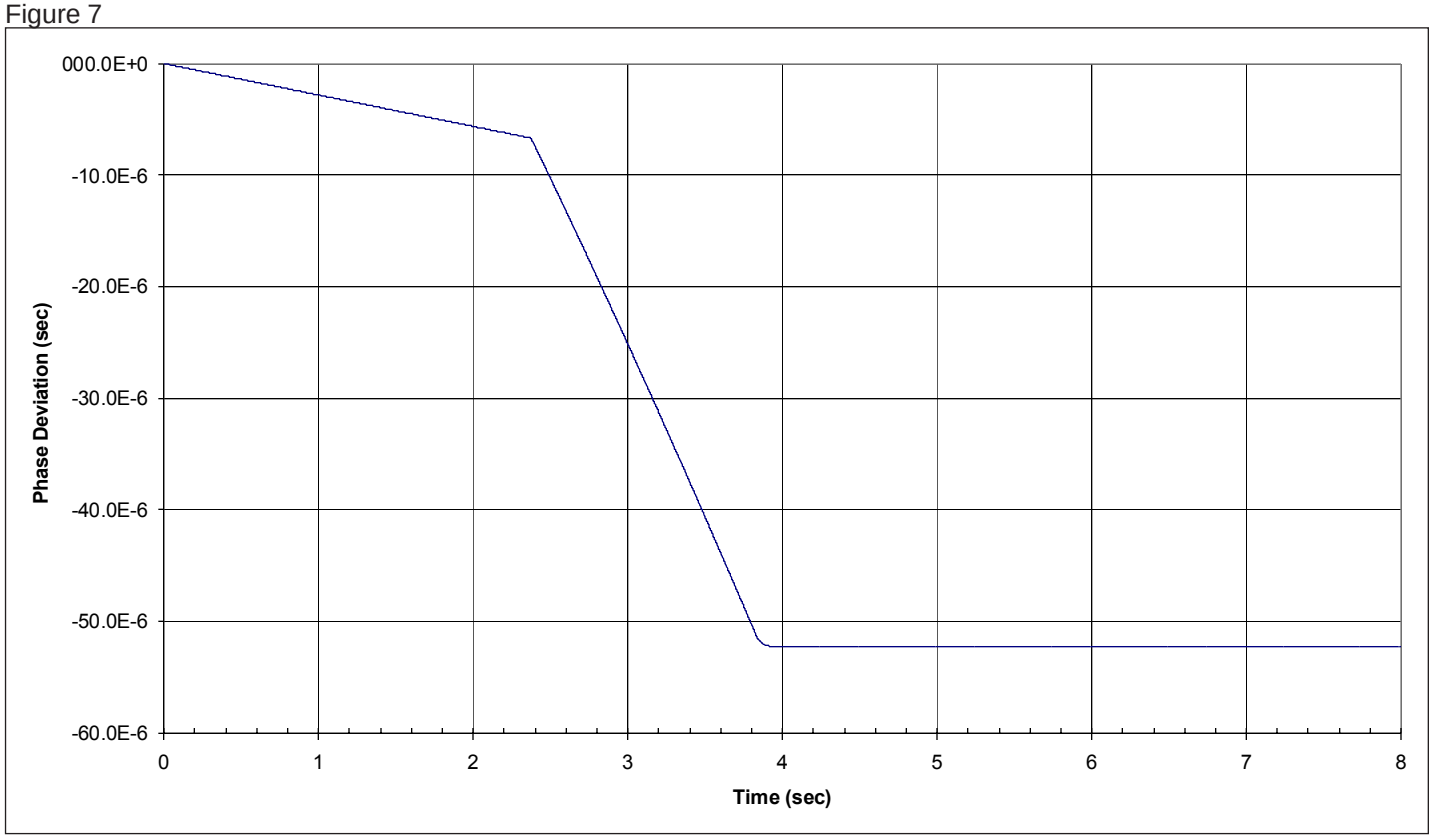
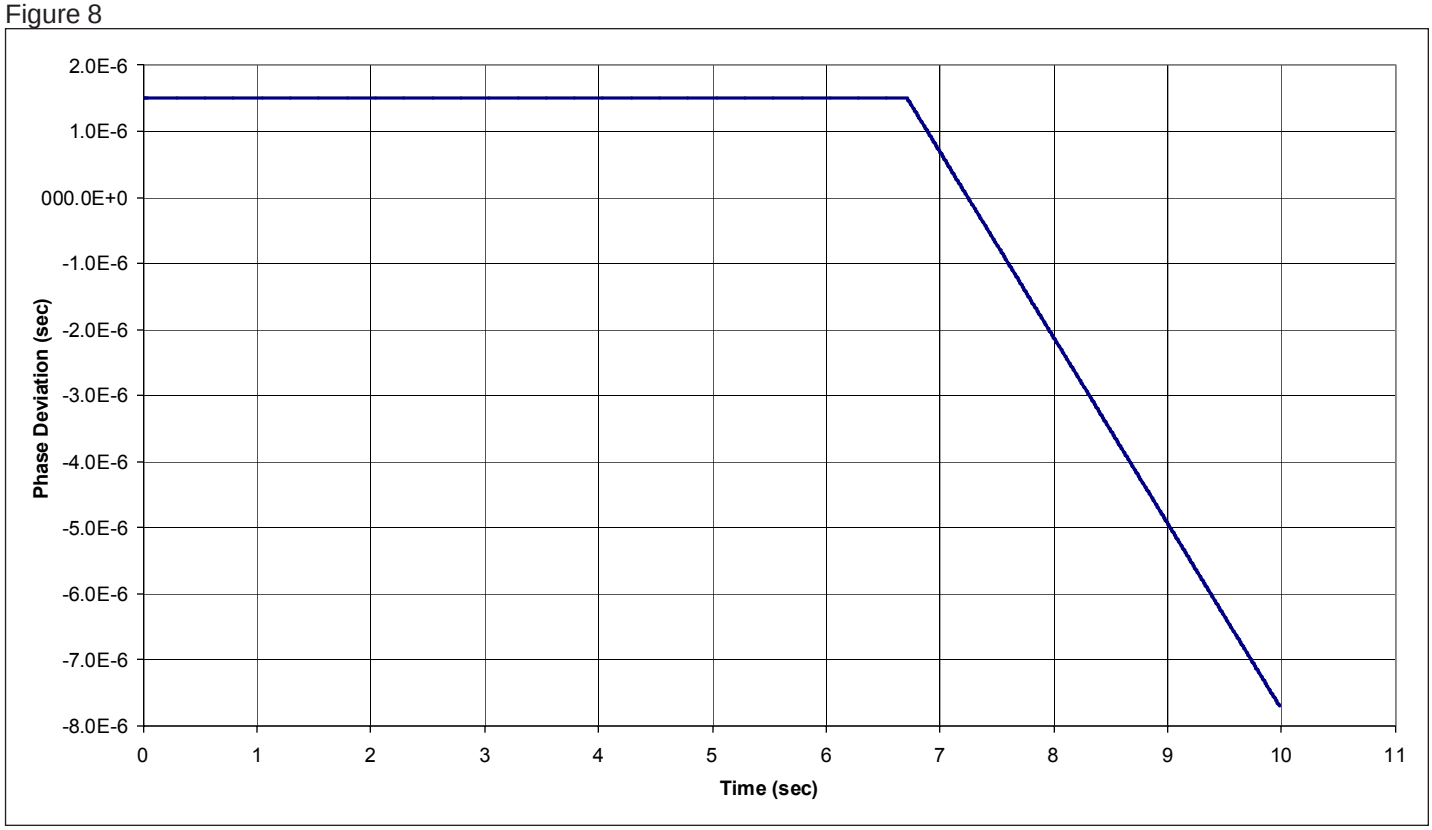
Switch from Free Run to a new Reference

Figure 7



Switch from a Reference to Free Run

Figure 8



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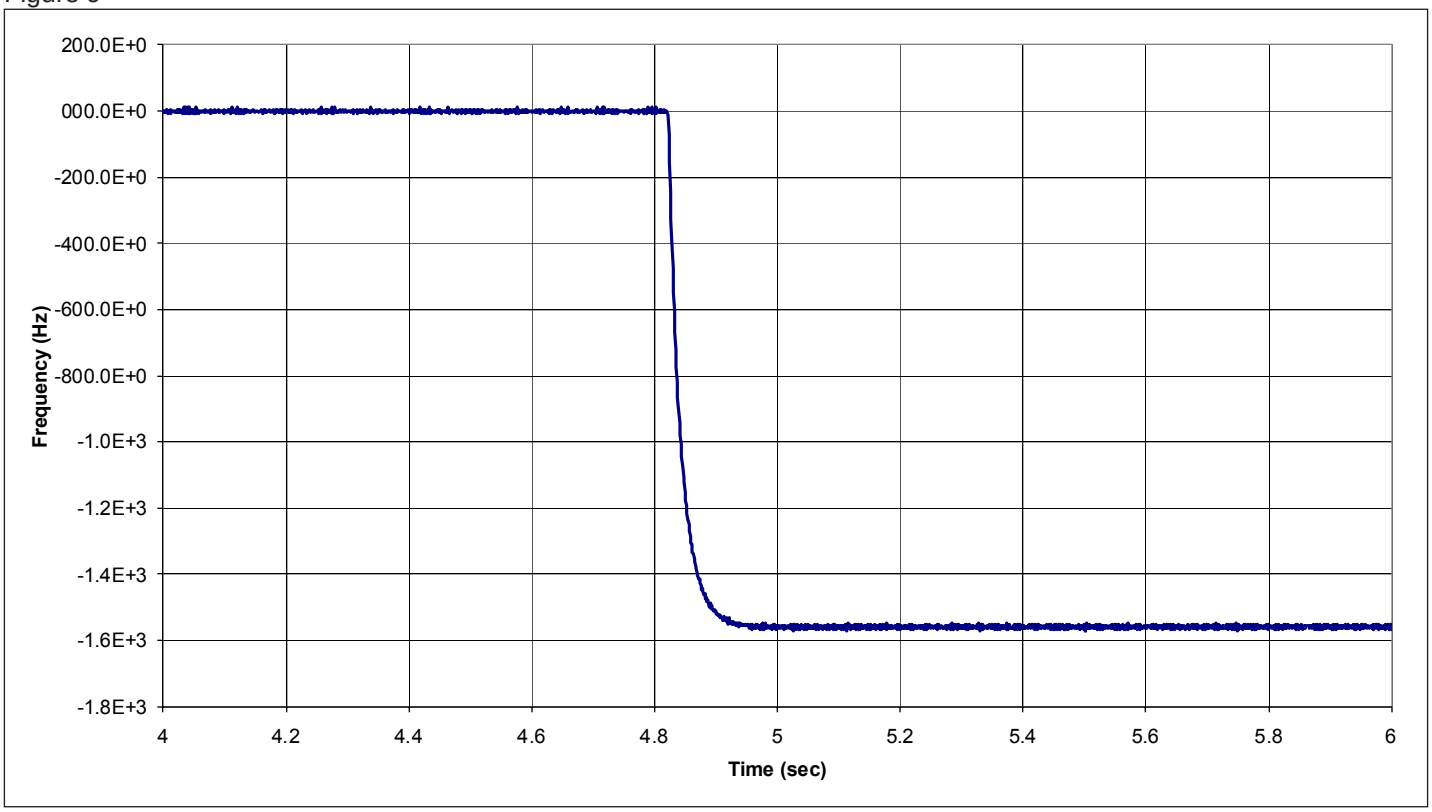
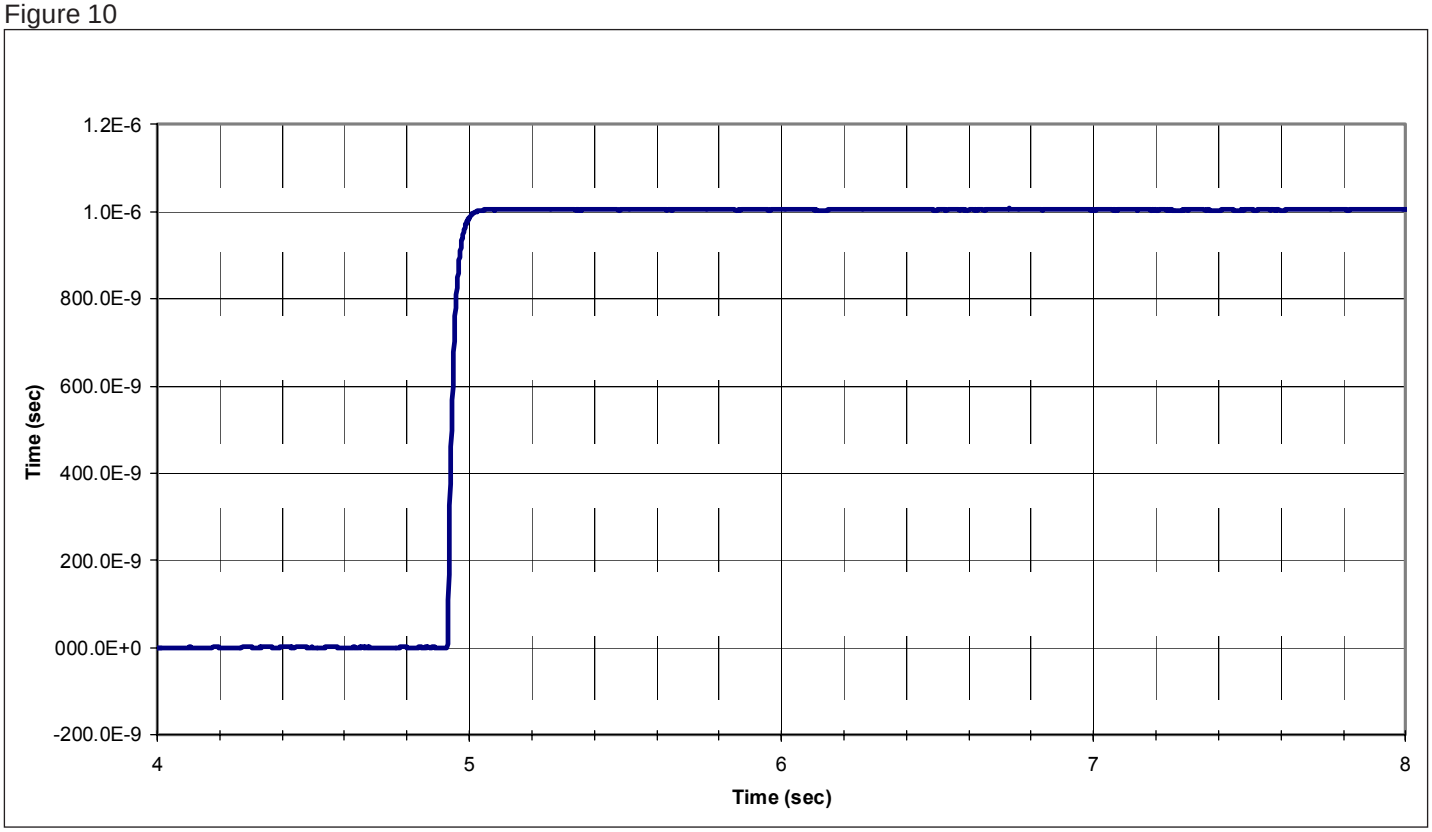
Step Response due to a -20ppm Freq. Step

Figure 9



1µs Phase Transient Response

Figure 10



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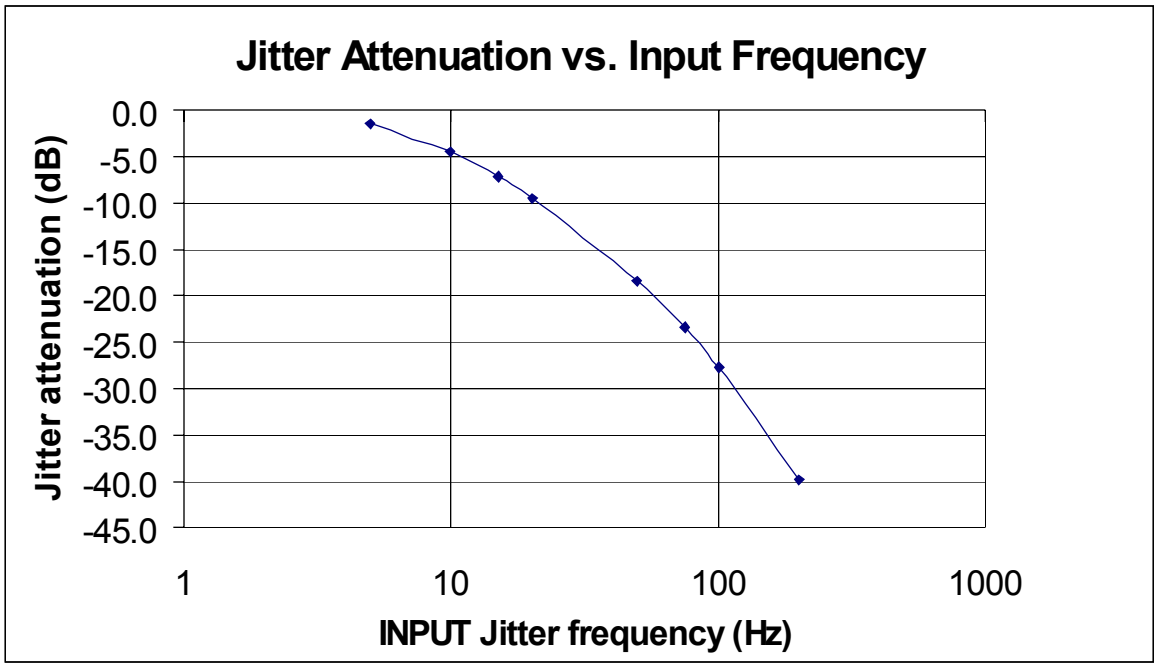
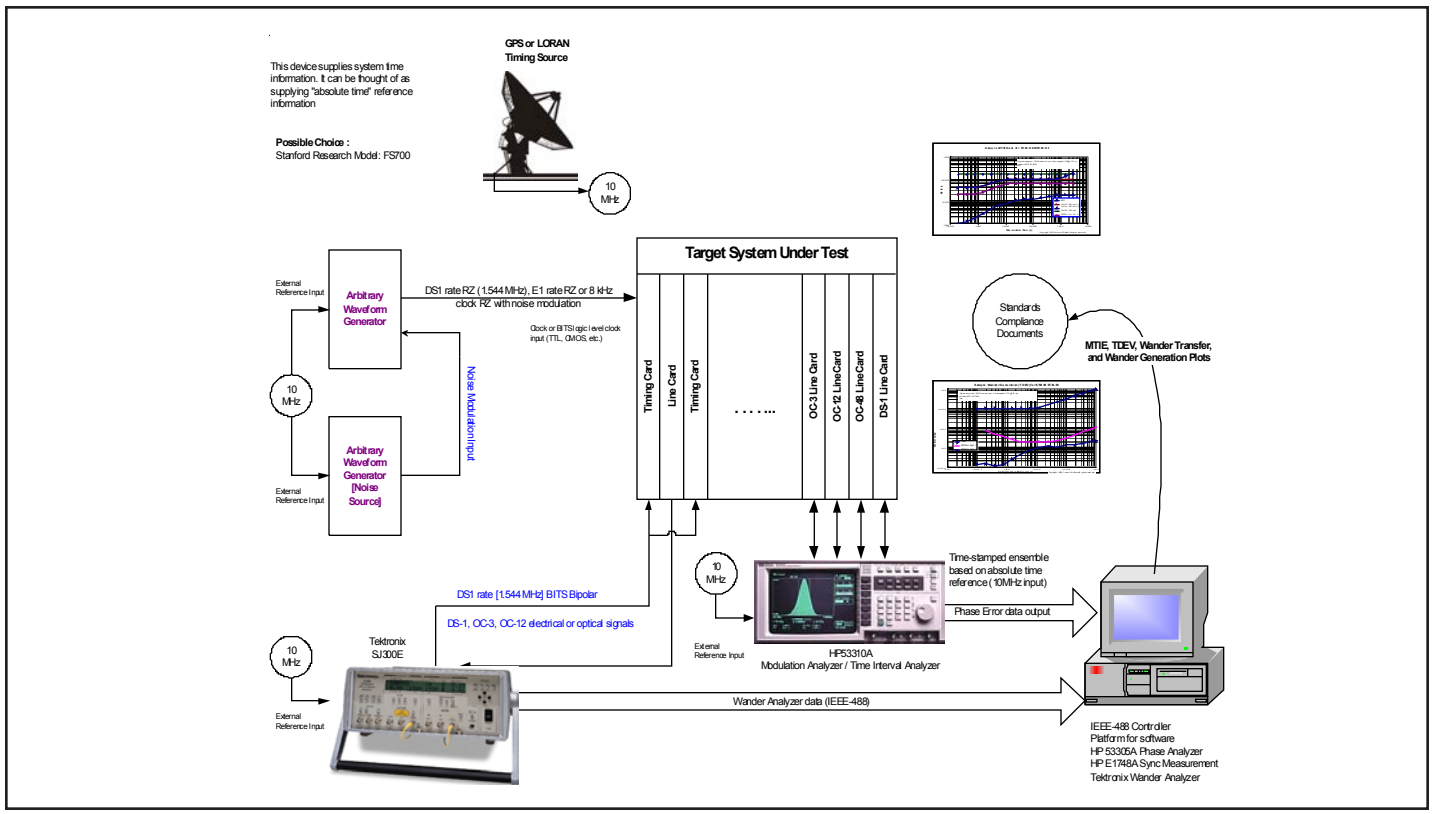
Jitter Attenuation

Figure 11



Typical System Test Setup

Figure 12



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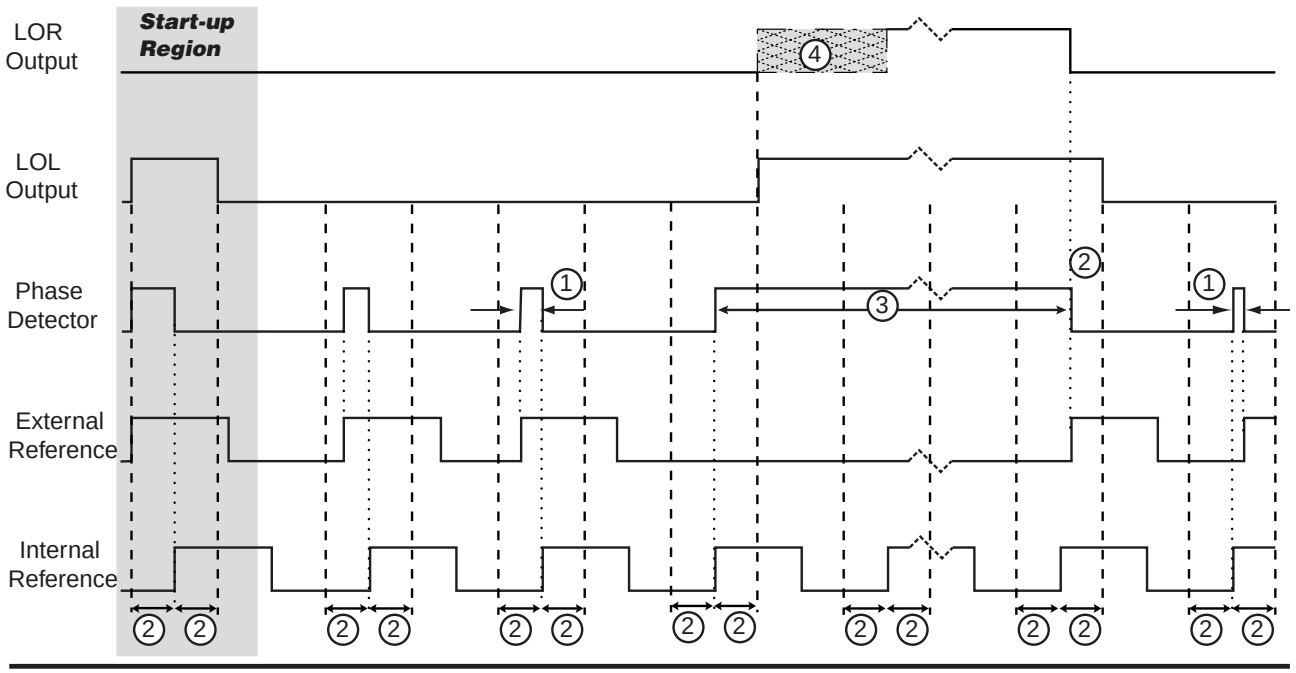
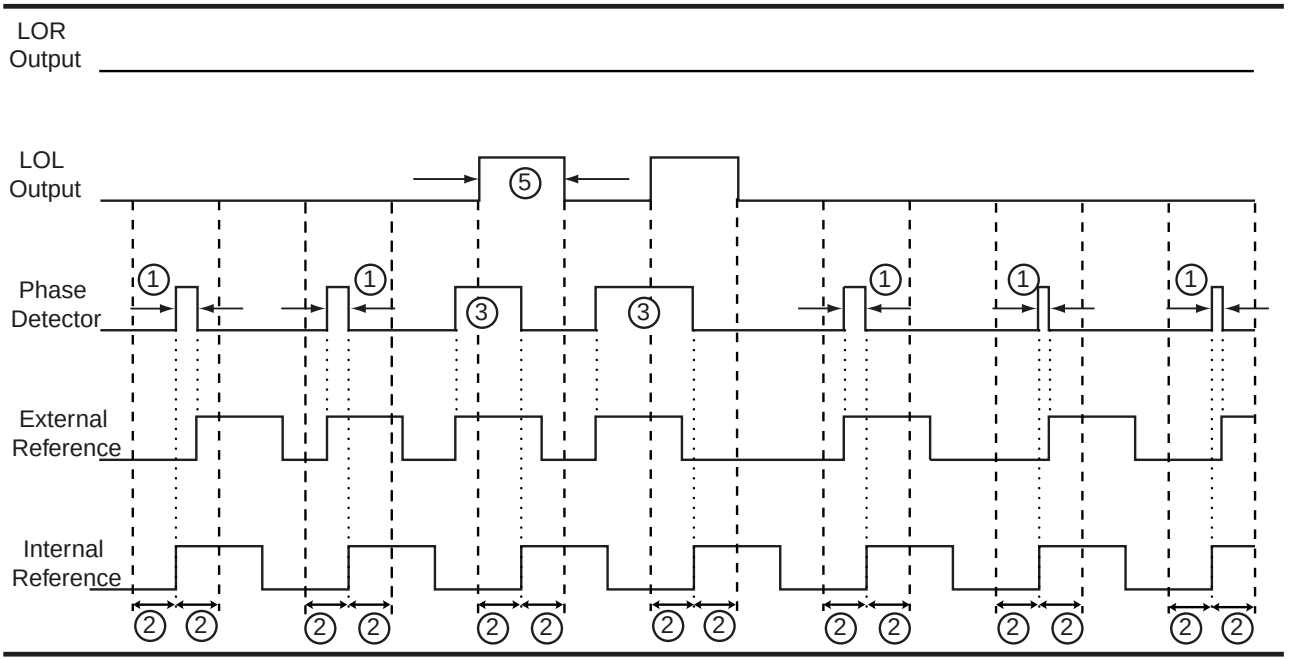
Alarm Timing Diagram

Figure 13





	8 kHz Reference Input Units
1	< 31.25 µsec
2	31.25 µsec
3	> 31.25 µsec
4	125 µsec wide range
5	Minimum pulse width = 62.5 µsec
Start-up Region	During Start-up, The LOL Alarm will pulse during the first second of operation

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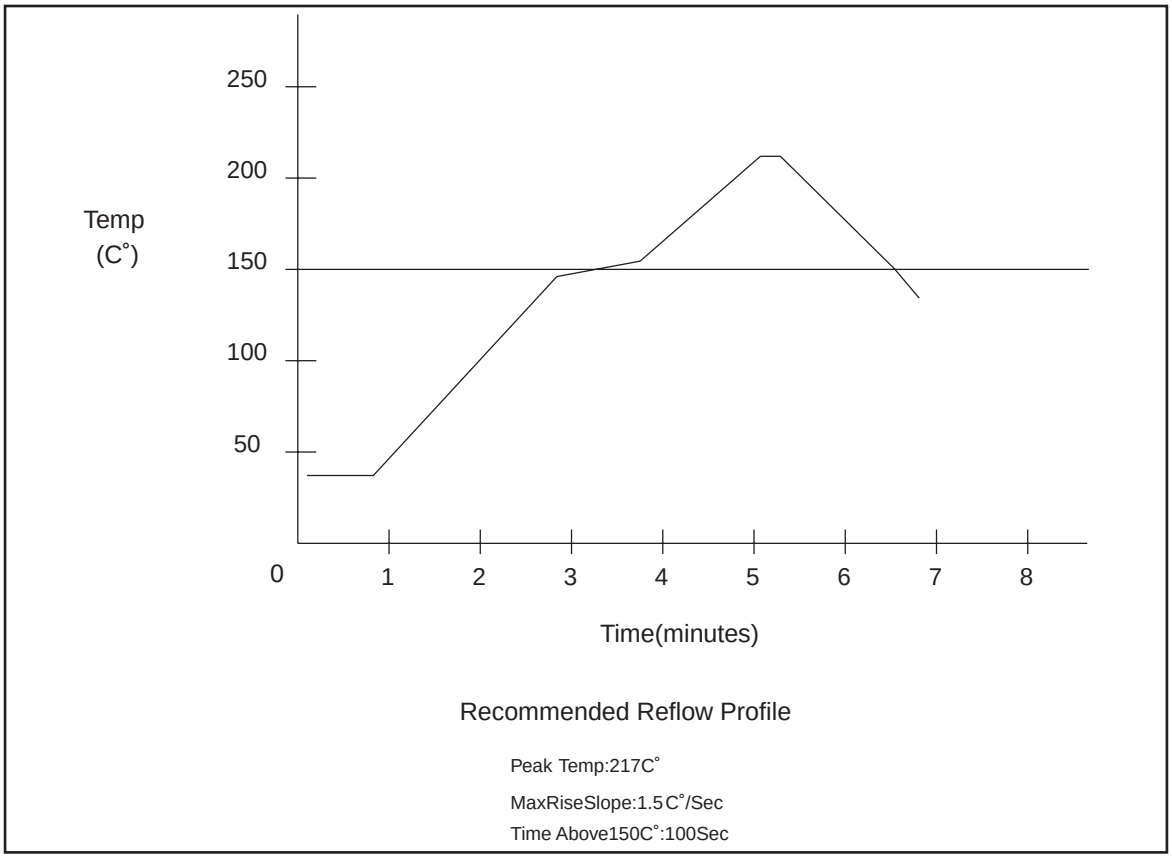
Solder Profile

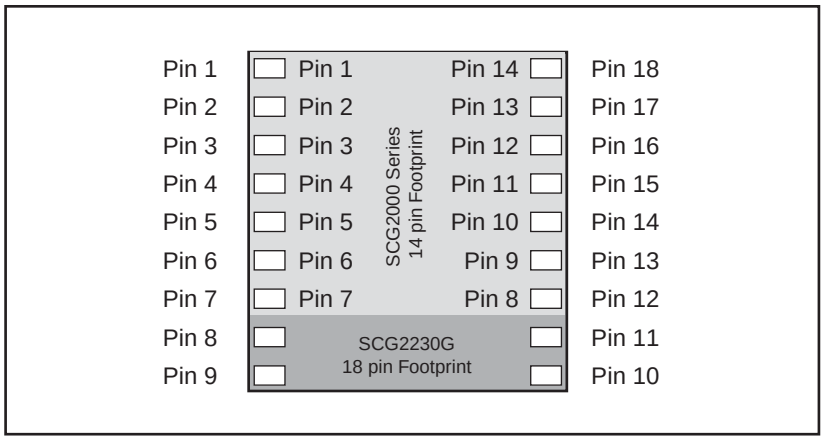
Figure 14



SCG2230G Footprint vs SCG2000 Series Footprint

Figure 15

SCG2230G is mechanically and functionally compatible with SCG2000 Series to allow use of either part. Refer to the SCG2000 Series data sheet for exact pin functions.



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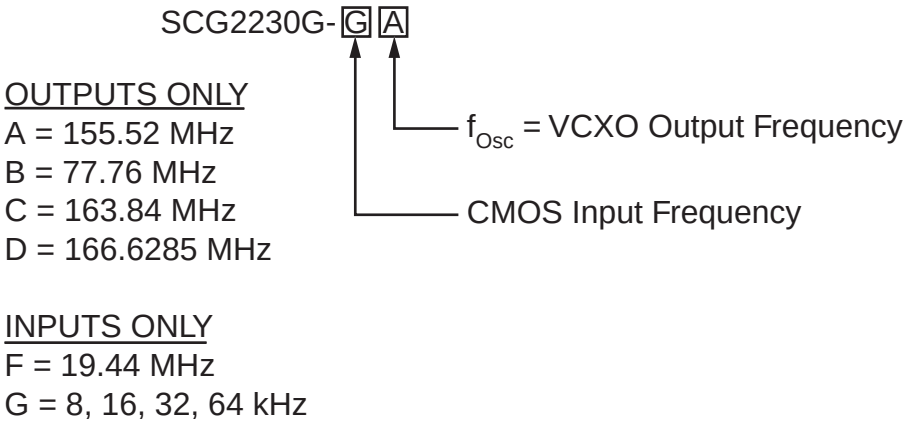

Ordering Information

Example: To order an SCG2230G with an LVPECL Output of 155.52 MHz and could use CMOS inputs of 8, 16, 32 or 64 kHz, Order part number SCG2230G-GA.

See Table 7 for other output frequencies based on the VCXO frequency, f_{OSC}.

See Table 9 for Input Reference Selection. Models that use 19.44 MHz as the Input Reference can only use a single reference frequency.

Please contact Connor-Winfield for other frequency configurations that may be available.

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Revision	Revision Date	Note
00	04/25/06	Product Release