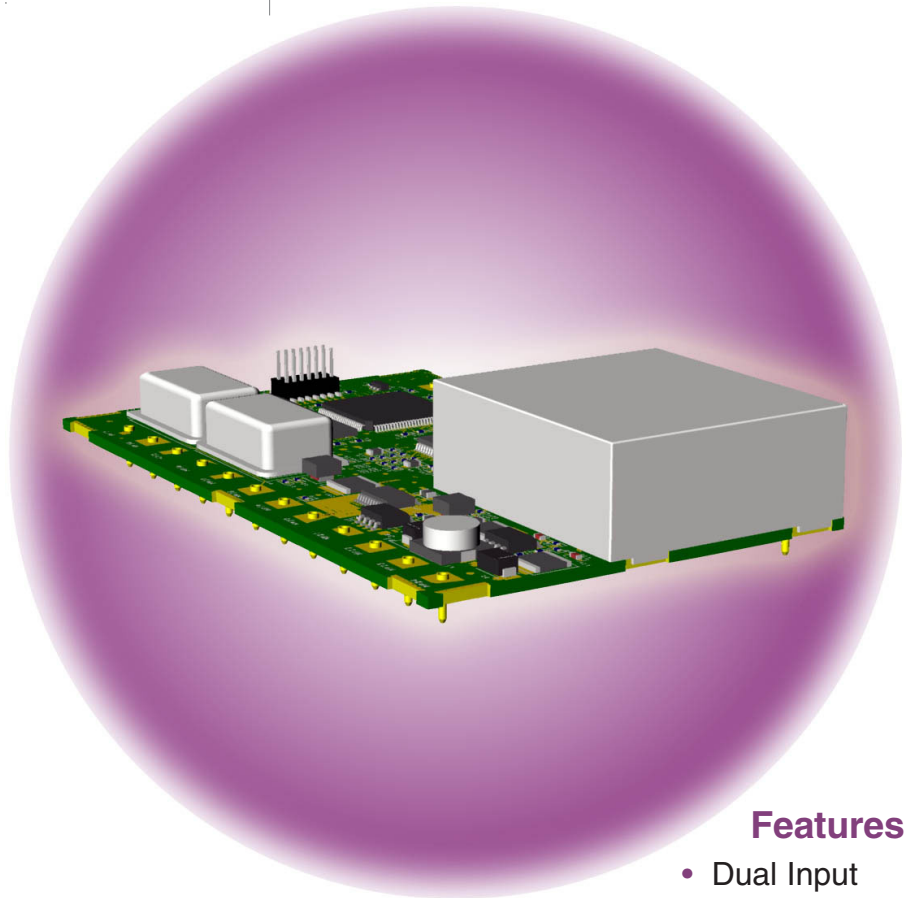


# Stratum 3E Timing Module (STM-S3E)



2111 Comprehensive Drive  
Aurora, Illinois 60505  
Phone: 630-851-4722  
Fax: 630-851-5040  
[www.conwin.com](http://www.conwin.com)



## Application

The Connor-Winfield Stratum 3E Simplified Control Timing Module acts as a complete system clock module for Stratum 3E timing applications in accordance with GR-1244-CORE, Issue 2, GR-253-CORE, Issue 3, and ITU-T G.812, Option III.

Connor-Winfield's Stratum 3E Timing module helps reduce the cost of your design by minimizing your development time and maximizing your control of the system clock with our simplified design.

## Features

- Dual Input References
- Hitless Switch Over
- 1.544 MHz -38.88 MHz
- 8 kHz Output
- 12 ppb Composite Hold Over Mode
- Fast Acquisition Mode
- Hold Over Good Indicator
- Phase Buildout Indicator
- LOR Alarms
- Reference Frequency Limit Alarm

|           |                  |
|-----------|------------------|
| Bulletin  | <b>TM012</b>     |
| Page      | <b>1 of 16</b>   |
| Revision  | <b>P06</b>       |
| Date      | <b>20 MAY 02</b> |
| Issued By | <b>MBATTS</b>    |

## General Description

Connor-Winfield's STM-S3E timing module provides Stratum 3E synchronization for a complete system clock solution in a single module in accordance with GR-1244-CORE Issue 2, GR-253-CORE Issue 3, and ITU-T G.812 Option III. The STM-S3E provides a reliable network element clock reference to line cards used in TDM, PDH, SONET, and SDH application environments. Typical applications include digital cross talks, DSLAMs, ADMs, multiservice platforms, switches and routers.

The STM-S3E meets 12 ppb Hold Over requirements over 0° – 70°C temperature range. The 5V power requirement will draw a maximum of 1.2 A during an initial start-up period and then drop to a typical current of 800 mA during normal operating conditions. It accepts two 8 kHz input references and can be manufactured to supply a fixed frequency from 1.544 MHz to 38.88 MHz.

The STM-S3E offers 4 user selectable modes of operation, Reference 1, Reference 2, Hold Over and Free Run. Mode of operation is selected by two control pins (Table 6). The current mode of operation is also indicated by two status pins (Table 7). Free Run is the default mode if no control signals are asserted on the control pins.

Reference 1 mode and Reference 2 mode are the two primary operating modes. When the module is locked to a valid reference, any time after initial power up or reset, the module is considered to be in the normal operating mode. During normal operation the output frequency is phase locked to the input reference frequency. The offset between the input and output is dependant upon the amount of noise that is present on the reference signal. For input tolerances, refer to Table 4.

Hold Over mode provides a stable frequency that is guaranteed to be within  $\pm 0.012$  ppm over the entire temperature range for the first 24 hours after entry into Hold Over. Hold Over is valid 701 seconds after a reference is selected and continues to do a running average every 8 seconds for the next 1049 seconds. Long-term Hold Over values are based on a 1049 second moving window average. Hold Over values are not updated during LOR or during Fast Acquisition mode. Hold Over values are buffered for at least 32 seconds to allow enough time to respond to the RFL alarm.

Free Run is a mode of operation in which the module is not locked to a reference and its output frequency is solely dependent on the initial frequency setting of the internal oscillator. The output frequency in Free Run is guaranteed to be  $\pm 4.6$  ppm of the nominal frequency.

A fifth, automatic mode of operation is Fast Acquisition mode. Fast Acquisition mode is entered whenever Reference 1 or 2 has been selected. After a new reference has been selected, the module uses internal filtering that limits the frequency movement to less than 2.9 ppm/sec. By 600 seconds the module switches to a slower 0.001Hz filter. While in normal mode, if the phase error is greater than 20  $\mu$ s, Fast Acquisition mode will be initiated. Fast Acquisition mode is further described as fast start mode in GR-1244-CORE, Issue 3, sec 3.6.

The STM-S3E may be reset by asserting a logic low signal

to the Reset pin or cycling the power. Using the Reset pin for a manual reset is the recommend method for resetting the module. Resetting the module by cycling the power requires more time due to the restablization of the internal ovenized oscillator.

The STM-S3E provides the user with non-interruptive Tri-State capabilities. By asserting a logic high signal to the Tri-State pin, the user is able to Tri-State all outputs. While in Tri-State, the module continues normal operations and accepts all normal inputs. When the module is released from Tri-State, all output signals are valid.

The STM-S3E module provides three output frequencies. The Sync\_Out is the primary synchronized output. It is phase locked to the input reference during normal operation and is set to a fixed frequency when operating in Hold Over or Free Run. Clock\_Out provides a frequency output that comes from an independent, undisciplined, free running oscillator that is  $\pm 4.6$  ppm from the nominal frequency. This output is typically used for reference frequency qualification. The 8 kHz output is derived from the Sync\_Out output.

The STM-S3E module provides a variety of alarm indicators to alert the user to multiple conditions that may affect the overall performance of their system. The LOR (Loss of Reference) alarm indicates that the active reference has been lost. RFL (Reference Frequency Limit) indicates that the Sync\_Out frequency is 15 ppm or more from the Free Run frequency. The PBO (Phase Build Out) pin indicates that a phase transient greater than 3.4  $\mu$ s over any 0.1 second interval has occurred. The PBO indicator will remain high as long as the phase transient condition exists.

The Mode Alarm pin is used to indicate that the module is not in a normal operating mode. Conditions that will cause the Mode Alarm to go high are Hold Over, Free Run, Fast Acquisition Modes or when Phase Build Out has been active for more than 0.4 seconds. During the latter condition, both the Mode Alarm indicator and the PBO indicator will be high. See Table 8 for a full description of input control pins and output indicator pins.

The Hold Over Good pin indicates that an initial average has been acquired to provide a qualified Hold Over frequency. The module requires approximately 700 seconds from any reference switch or mode switch to a new reference to reacquire a valid average before the indicator goes high (Fig. 17). Initially, entry into Hold Over prior to this will result in a Free Run frequency. After the first Hold Over Good indication, entry into Hold Over will be the last valid Hold Over frequency.

The STM-S3E meets the requirements for wander generation and wander transfer as required by GR-1244, sections 5.3 and 5.4. Figures 4, 5 and 6 show typical results. It also complies with phase transient requirements during Reference Rearrangement, Entry into Hold Over, and 1  $\mu$ s transient. See figures 7-9 for typical performance results and requirement masks. Input jitter is attenuated at about 20 dB/decade to minimize jitter noise from being passed to other network elements or clocks. Figure 10 illustrates the STM-S3E's typical roll off of attenuated jitter.

Table 1

## Absolute Maximum Rating

| Symbol   | Parameter                           | Minimum | Nominal | Maximum | Units  | Notes |
|----------|-------------------------------------|---------|---------|---------|--------|-------|
| $V_{CC}$ | Power Supply Voltage                | -0.5    |         | 5.5     | Volts  | 1.0   |
| $V_I$    | Input Voltage                       | -0.5    |         | 5.5     | Volts  | 1.0   |
| $T_s$    | Storage Temperature                 | -40     |         | 85      | deg. C | 1.0   |
| $V_{TS}$ | Voltage Applied to Tri-State Output | -0.5    |         | 5.5     | Volts  |       |

Table 2

## Recommended Operating Conditions

| Symbol   | Parameter                       | Minimum | Nominal | Maximum | Units | Notes |
|----------|---------------------------------|---------|---------|---------|-------|-------|
| $V_{CC}$ | Power Supply Voltage            | 4.75    |         | 5.25    | Volts |       |
| $V_{IH}$ | High level input voltage - CMOS | 2.0     |         | 5.25    | Volts | 2.0   |
| $V_{IL}$ | Low level input voltage - CMOS  | 0       |         | 0.8     | Volts |       |

Table 3

## DC Characteristics

| Symbol   | Parameter                                                                       | Minimum | Nominal | Maximum | Units | Notes |
|----------|---------------------------------------------------------------------------------|---------|---------|---------|-------|-------|
| $V_{OH}$ | High level output voltage,<br>$I_{OH} = -4.0\text{mA}$ , $V_{CC} = \text{min.}$ | 2.4     | 3.3     | 3.6     | Volts | 3.0   |
| $V_{OL}$ | Low level output voltage,<br>$I_{OL} = 8.0\text{mA}$ , $V_{CC} = \text{max.}$   |         |         | 0.4     | Volts |       |

Table 4

## Specifications

| Parameter                                     | Specifications                                 | Notes |
|-----------------------------------------------|------------------------------------------------|-------|
| Frequency Range (Sync_Out)                    | 1.544 MHz - 38.88 MHz                          |       |
| Frequency Range (Clk_Out)                     | 1.544 MHz - 51.84 MHz                          |       |
| Supply Current                                | 800 mA typical, 1.2 A during warm-up (Maximum) |       |
| Timing Reference Inputs                       | GR-1244-CORE 3.2.1                             |       |
| Jitter, Wander and Phase Transient Tolerances | GR-1244-CORE 4.2-4.4, GR-253-CORE 5.4.4.3.6    |       |
| Wander Generation                             | GR-1244-CORE 5.3, GR-253-CORE 5.4.4.3.2        |       |
| Wander Transfer                               | GR-1244-CORE 5.4                               |       |
| Jitter Generation                             | GR-1244-CORE 5.5, GR-253-CORE 5.6.2.3          |       |
| Jitter Transfer                               | GR-1244-CORE 5.5, GR-253-CORE 5.6.2.1          |       |
| Phase Transients                              | GR-1244-CORE 5.6, GR-253-CORE 5.4.4.3.3        |       |
| Sync_Out (Pin #15) Free Run Accuracy          | ±4.6 ppm over temperature range                |       |
| Clock_Out (Pin #18) Accuracy                  | ±4.6 ppm over temperature range                |       |
| Hold Over Stability                           | ±0.012 ppm                                     | 4.0   |
| Initial Offset                                | ±0.001 ppm                                     |       |
| Temperature                                   | ±0.010 ppm                                     |       |
| Drift                                         | ±0.001 ppm                                     |       |
| Maximum Hold Over History                     | 1049 seconds                                   |       |
| Minimum Time for Hold Over                    | 701 seconds after a reference rearrangement    |       |
| Pull-in/ Hold-in Range                        | ±17 ppm from Free Run frequency                | 5.0   |
| Lock Time                                     | 700 sec.                                       |       |
| Lock Accuracy                                 | 0.001 ppm (GR-1244-CORE 2.8)                   | 6.0   |
| RFL Alarm Limit                               | ±15 ppm from Free Run frequency                |       |

### NOTES:

1.0: Stresses beyond those listed under Absolute Maximum Rating may cause damage to the device. Operation beyond Recommended Conditions is not implied.

2.0: Inputs are 3.3V CMOS, 5V tolerant

3.0: Logic is 3.3V CMOS

4.0: Hold Over stability is the cumulative fractional frequency offset as described by GR-1244-CORE, 5.2

5.0: Pull-in Range is the maximum frequency deviation from nominal clock rate on the reference inputs to the timing module that can be overcome to pull into synchronization with the reference

6.0: After 700 seconds at stable temperature (±5° F)



## Pin Description

Table 5

| Pin # | Connection           | Description                                                                                                                                                                           |
|-------|----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1     | Status 0             | Mode indicator.                                                                                                                                                                       |
| 2     | Status 1             | Mode indicator.                                                                                                                                                                       |
| 3     | LOR                  | Loss of Reference indicator. 1 = active reference has been lost.                                                                                                                      |
| 4     | PBO                  | Phase build out indicator. 1 = module is in a phase build out condition.                                                                                                              |
| 5     | GND                  | Ground                                                                                                                                                                                |
| 6     | 8 kHz Output         | Derived from Sync_Out.                                                                                                                                                                |
| 7     | Reset                | Master reset for the module. A low pulse will reset the module. A logic low for a minimum of 1 $\mu$ s is recommended to ensure a complete reset. This pin is pulled high internally. |
| 8     | Tri-State            | Tri-State control for all outputs. 1 = Hi-Z condition, 0 = Normal operation. Pin is pulled low internally.                                                                            |
| 9     | Hold Over Good       | Indicates that the module has acquired enough data to provide an average Hold Over value.                                                                                             |
| 10    | Mode Alarm           | Alarm indicator output. 1 = Alarm condition, 0 = Normal operation.                                                                                                                    |
| 11    | CNTL A               | Mode control input. Pin is pulled low internally.                                                                                                                                     |
| 12    | CNTL B               | Mode control input. Pin is pulled low internally.                                                                                                                                     |
| 13    | RFL                  | Reference frequency limit alarm for the phase locked loop. 1= Unit is $\pm 15$ ppm from Free Run freq.                                                                                |
| 14    | GND                  | Ground                                                                                                                                                                                |
| 15    | Sync_Out             | System clock output                                                                                                                                                                   |
| 16    | Future Use           | Reserved for future use. Do not assert this pin                                                                                                                                       |
| 17    | GND                  | Ground                                                                                                                                                                                |
| 18    | Clock_Out            | An independent, Stratum 3 clock output with the required $\pm 4.6$ ppm accuracy. May be used as general purpose clock                                                                 |
| 19    | Future Use           | Reserved for future use. Do not assert this pin                                                                                                                                       |
| 20    | GND                  | Ground                                                                                                                                                                                |
| 21    | External Reference 2 | External reference #2 input                                                                                                                                                           |
| 22    | GND                  | Ground                                                                                                                                                                                |
| 23    | External Reference 1 | External reference #1 input                                                                                                                                                           |
| 24    | +5 V <sub>DC</sub>   | +5 Volt DC supply                                                                                                                                                                     |

## Control Inputs

Table 6

| CNTL B | CNTL A | Mode Selected |
|--------|--------|---------------|
| 0      | 0      | Free Run      |
| 0      | 1      | Reference 1   |
| 1      | 0      | Reference 2   |
| 1      | 1      | Hold Over     |

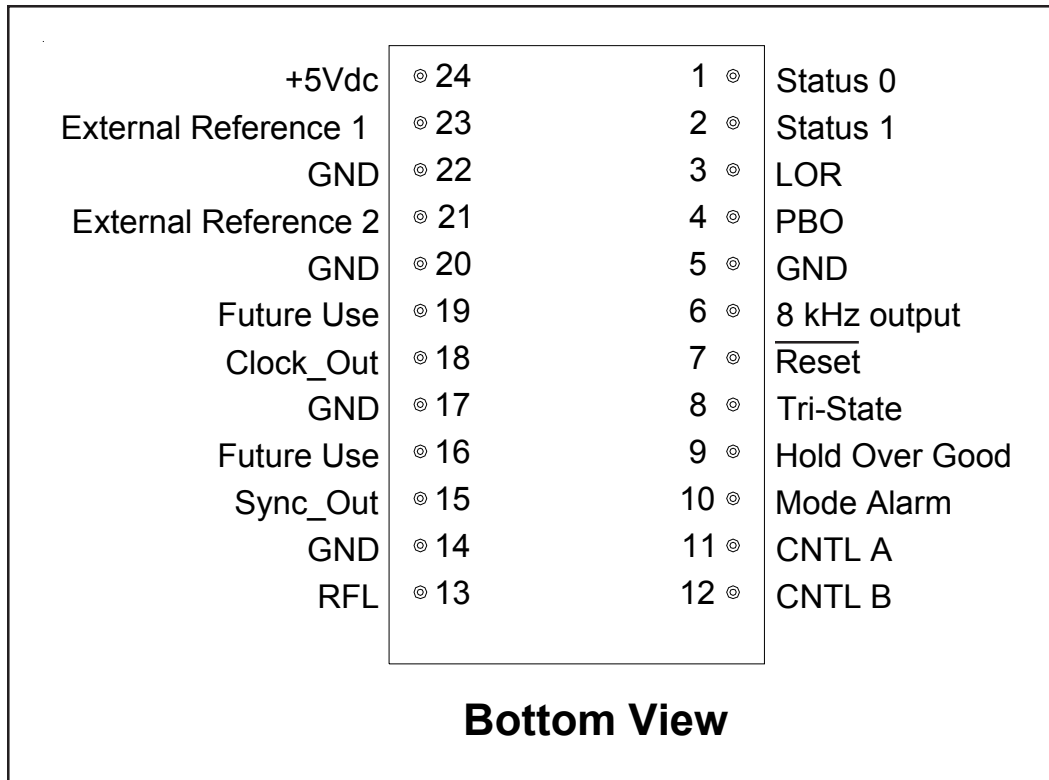
## Status Outputs

Table 7

| Status 1 | Status 0 | Mode        |
|----------|----------|-------------|
| 0        | 0        | Free Run    |
| 0        | 1        | Reference 1 |
| 1        | 0        | Reference 2 |
| 1        | 1        | Hold Over   |

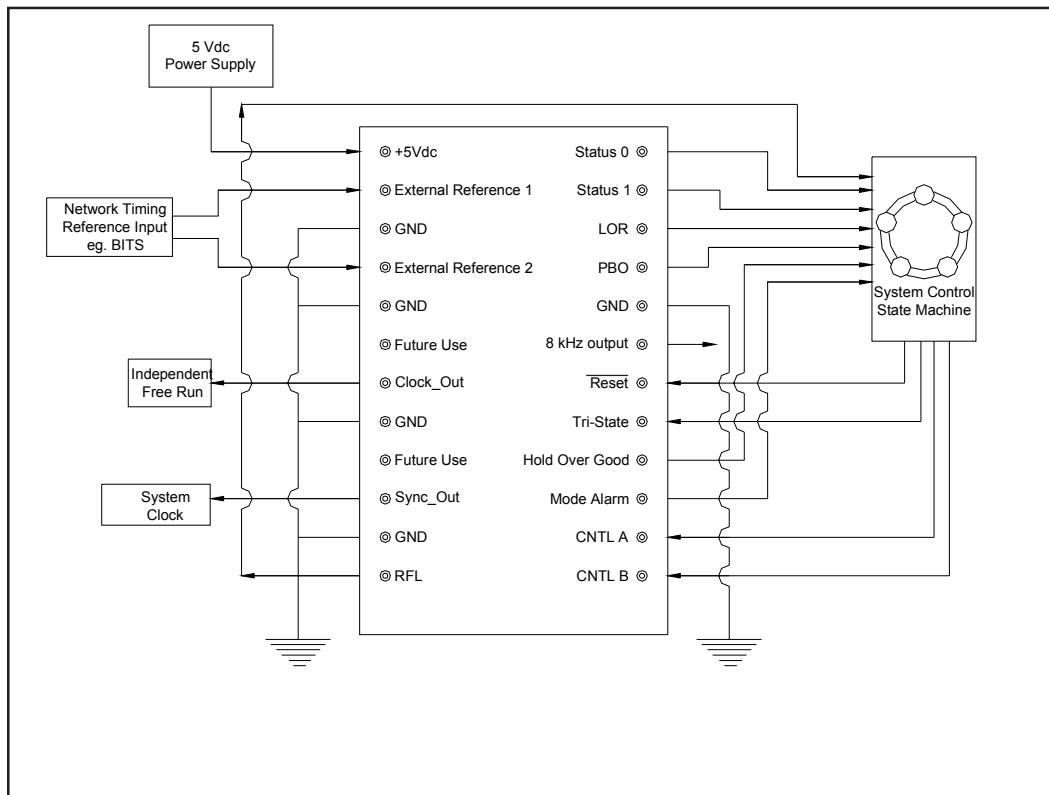
## Pin Assignment

Figure 1



## Typical Application Setup

Figure 2



## Functional Truth Table

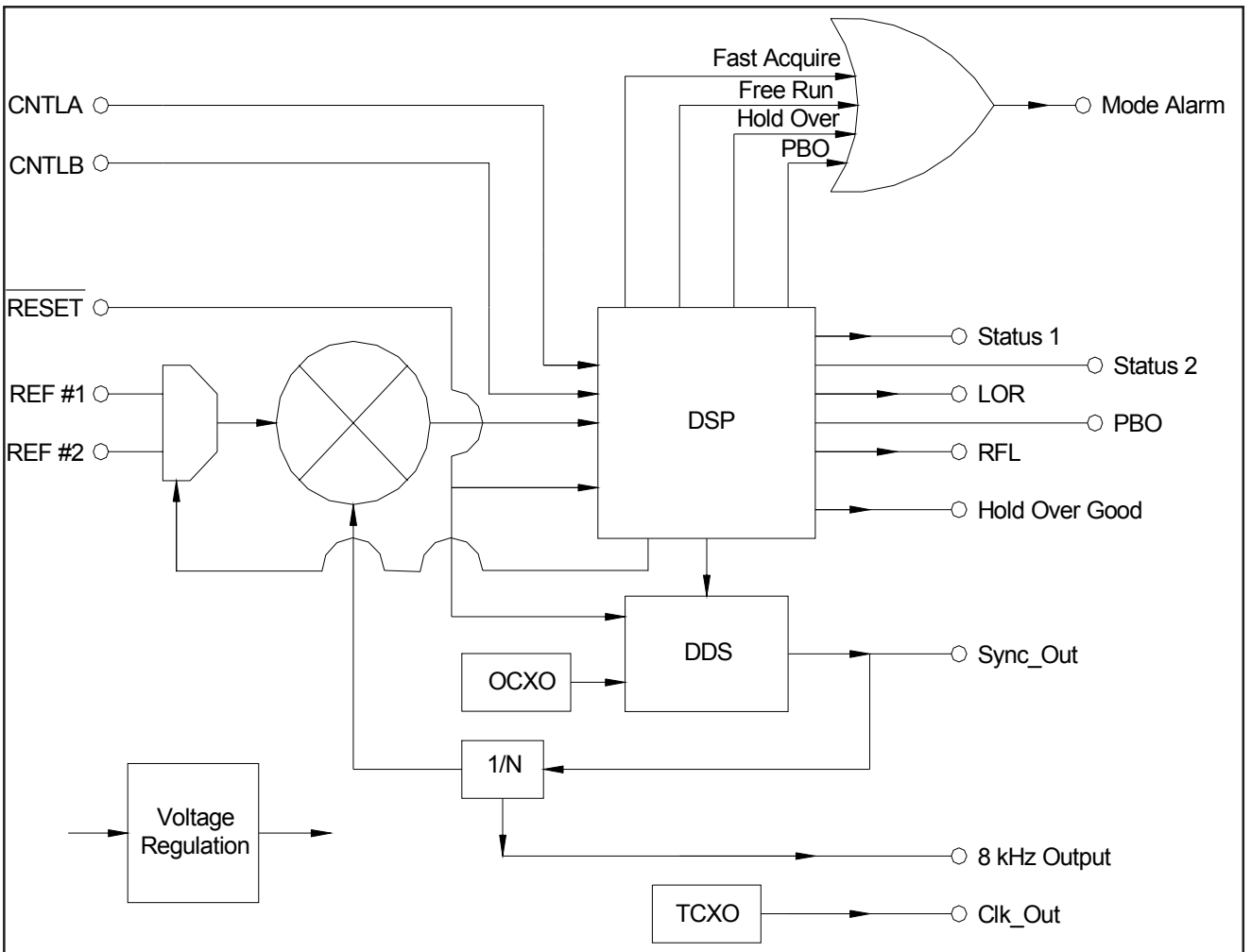
Table 8

| CNTLB | CNTLA | Mode         | Status1 | Status0 | Alarm | RFL | LOR | PBO | Condition                                                                                                                |
|-------|-------|--------------|---------|---------|-------|-----|-----|-----|--------------------------------------------------------------------------------------------------------------------------|
| 0     | 0     | Free Run     | 0       | 0       | 1     | 0   | 0   | 0   |                                                                                                                          |
| 0     | 0     | Free Run     | 0       | 0       | 1     | 1   | 0   | 0   |                                                                                                                          |
| 0     | 1     | Reference #1 | 0       | 1       | 0     | 0   | 0   | 0   | Normal Operation                                                                                                         |
| 0     | 1     | Reference #1 | 0       | 1       | 1     | 0   | 0   | 0   | Unit is in Fast Acquire mode                                                                                             |
| 0     | 1     | Reference #1 | 0       | 1       | 0     | 1   | 0   | 0   | Output freq. is 15 ppm or more from Free Run mode freq.                                                                  |
| 0     | 1     | Reference #1 | 0       | 1       | 0     | 0   | 1   | 0   | Selected reference signal is not detected and unit is in pseudo-Hold Over*                                               |
| 0     | 1     | Reference #1 | 0       | 1       | 0     | 0   | 0   | 1   | Phase build-out is occurring on selected reference                                                                       |
| 0     | 1     | Reference #1 | 0       | 1       | 1     | 0   | 0   | 1   | Phase build-out is occurring and has continuously occurred for at least 0.4 seconds and the unit is in pseudo-Hold Over* |
| 1     | 0     | Reference #2 | 1       | 0       | 0     | 0   | 0   | 0   | Normal Operation                                                                                                         |
| 1     | 0     | Reference #2 | 1       | 0       | 1     | 0   | 0   | 0   | Unit is in Fast Acquire mode                                                                                             |
| 1     | 0     | Reference #2 | 1       | 0       | 0     | 1   | 0   | 0   | Output freq. is 15 ppm or more from Free Run mode freq.                                                                  |
| 1     | 0     | Reference #2 | 1       | 0       | 0     | 0   | 1   | 0   | Selected reference signal is not detected and unit is in pseudo-Hold Over*                                               |
| 1     | 0     | Reference #2 | 1       | 0       | 0     | 0   | 0   | 1   | Phase build-out is occurring on selected reference                                                                       |
| 1     | 0     | Reference #2 | 1       | 0       | 1     | 0   | 0   | 1   | Phase build-out is occurring and has continuously occurred for at least 0.4 seconds and the unit is in pseudo-Hold Over* |
| 1     | 1     | Hold Over    | 1       | 1       | 1     | 0   | 0   | 0   |                                                                                                                          |
| 1     | 1     | Hold Over    | 1       | 1       | 1     | 1   | 0   | 0   |                                                                                                                          |

\*Pseudo-Hold Over is a condition when the module is no longer tracking a reference and is holding the last output that was sent to the Sync\_Out pin. Variations in the output frequency are due only to the drift of the OCXO.

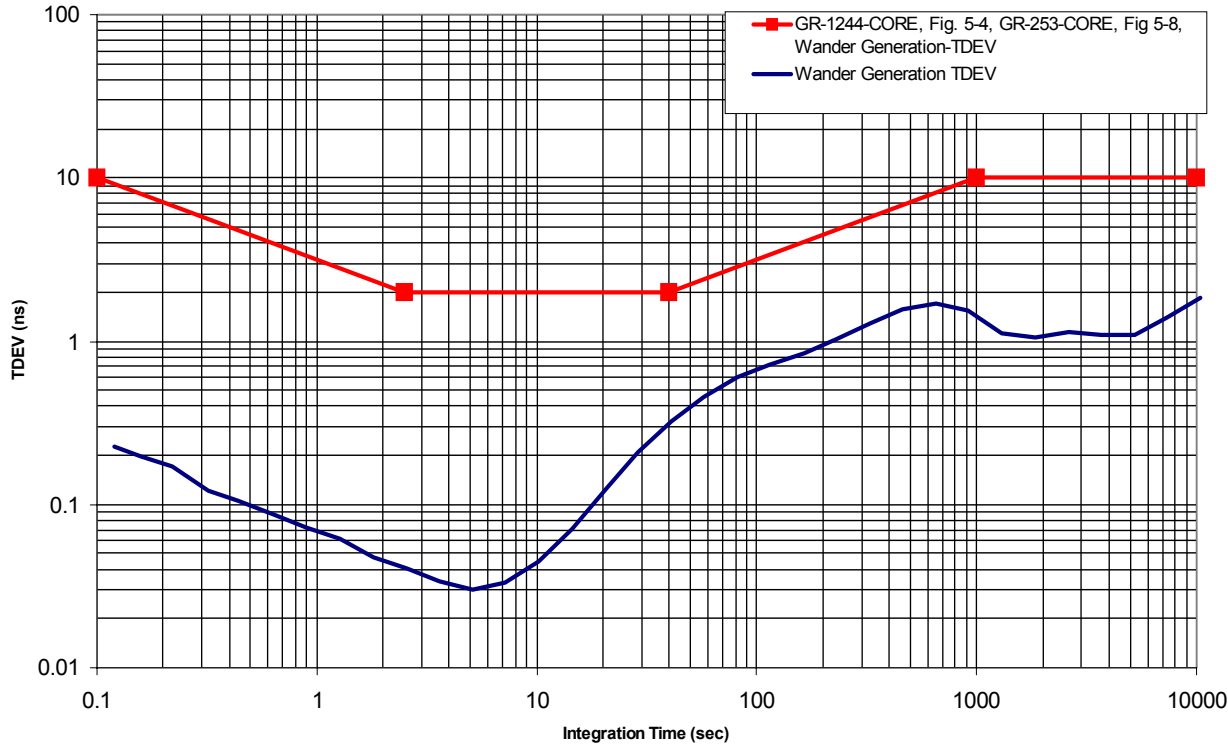
## Functional Block Diagram

Figure 3



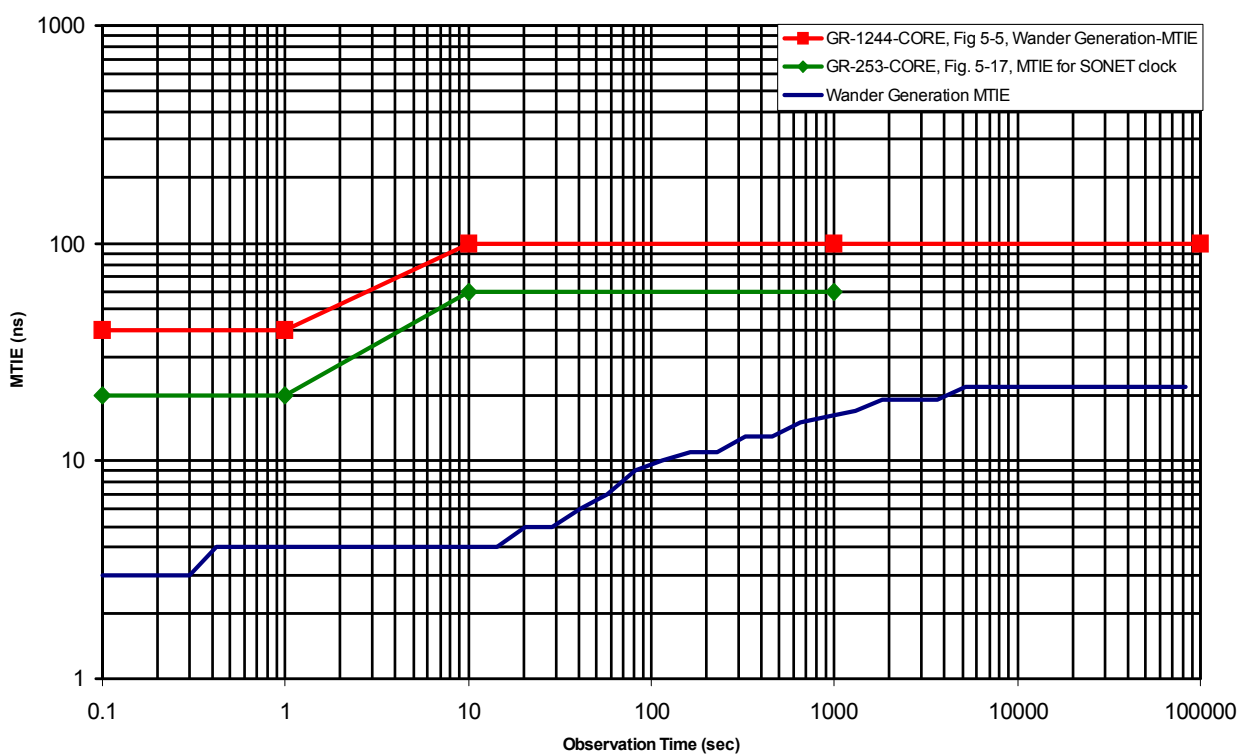
### 3E Wander Generation TDEV

Figure 4



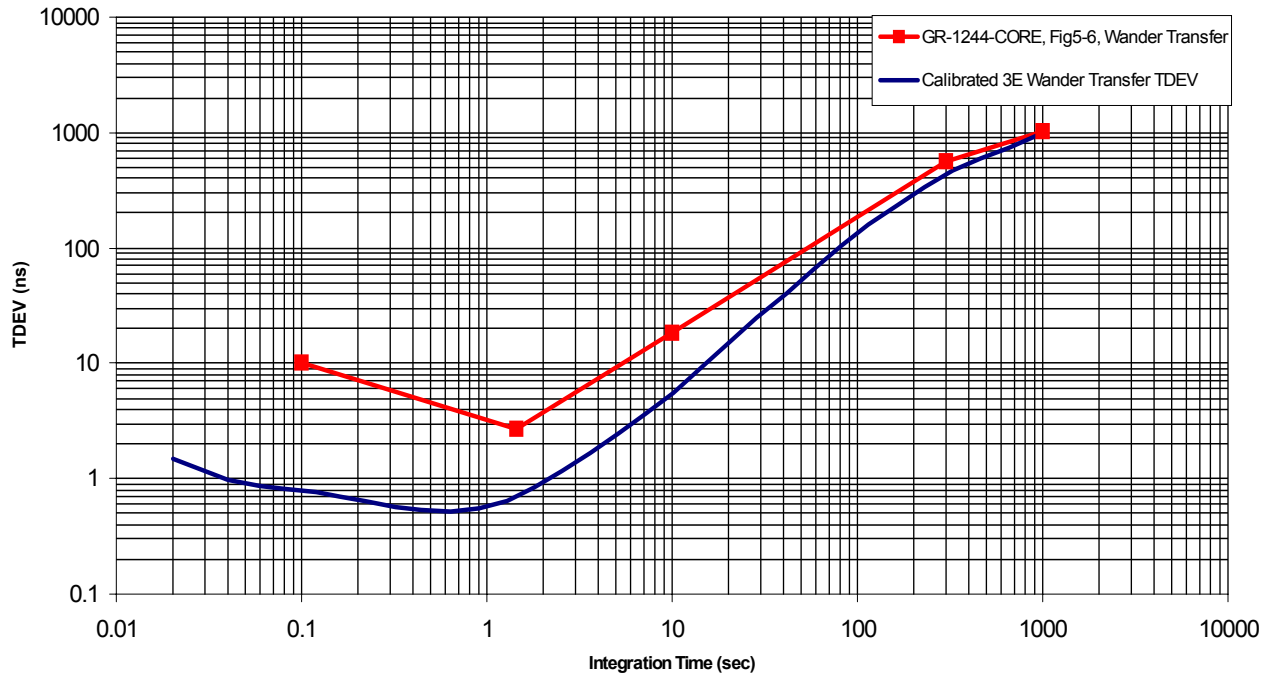
### 3E Wander Generation MTIE

Figure 5



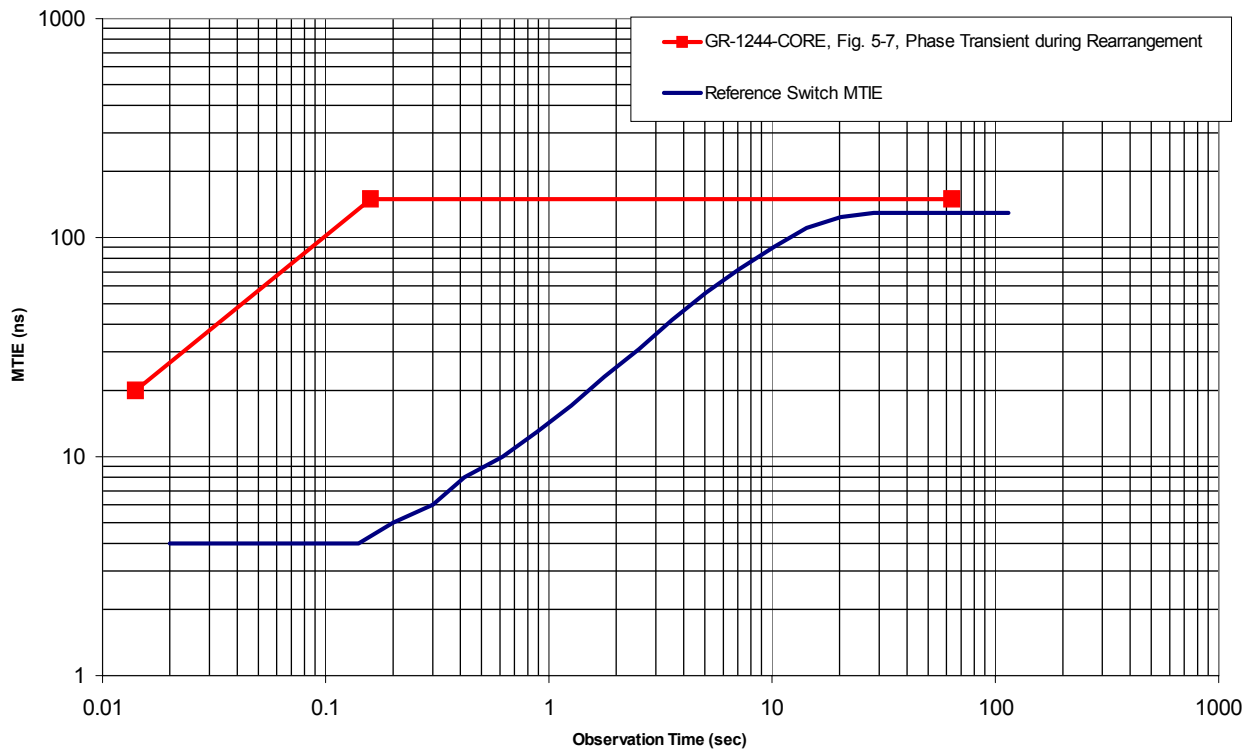
## 3E Wander Transfer TDEV

Figure 6



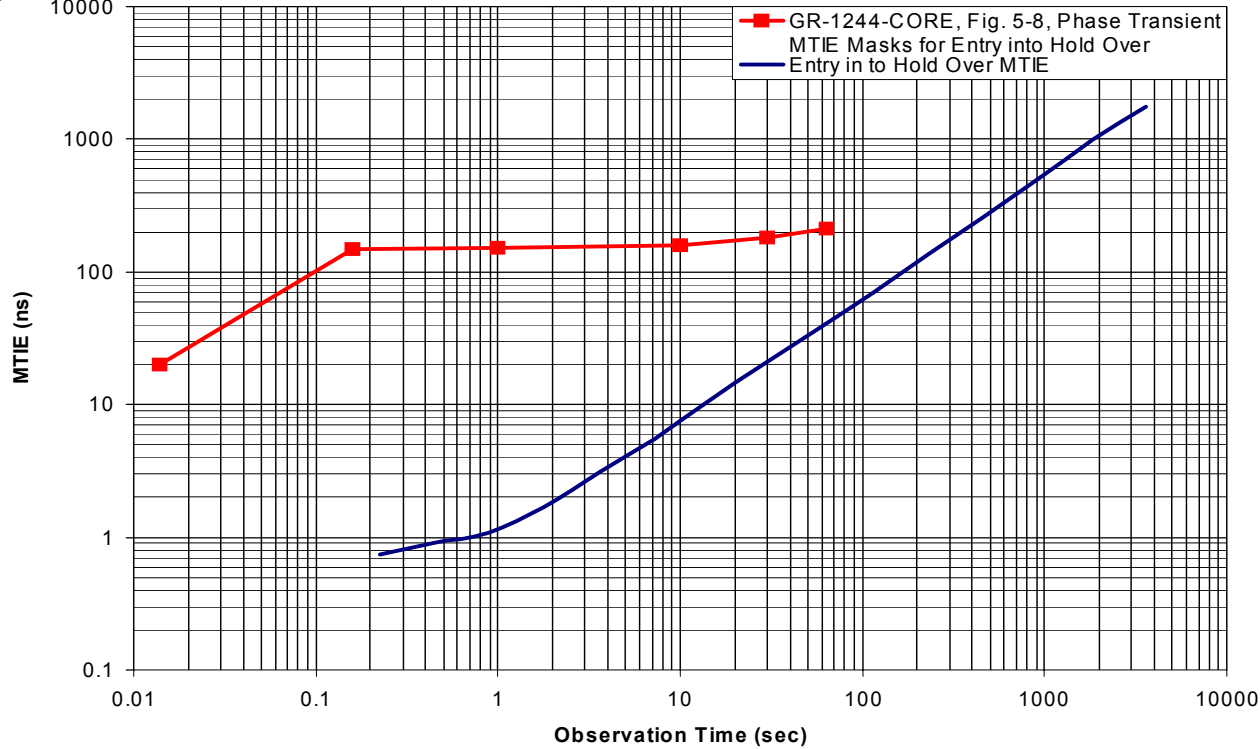
## 3E MTIE During Reference Rearrangement

Figure 7



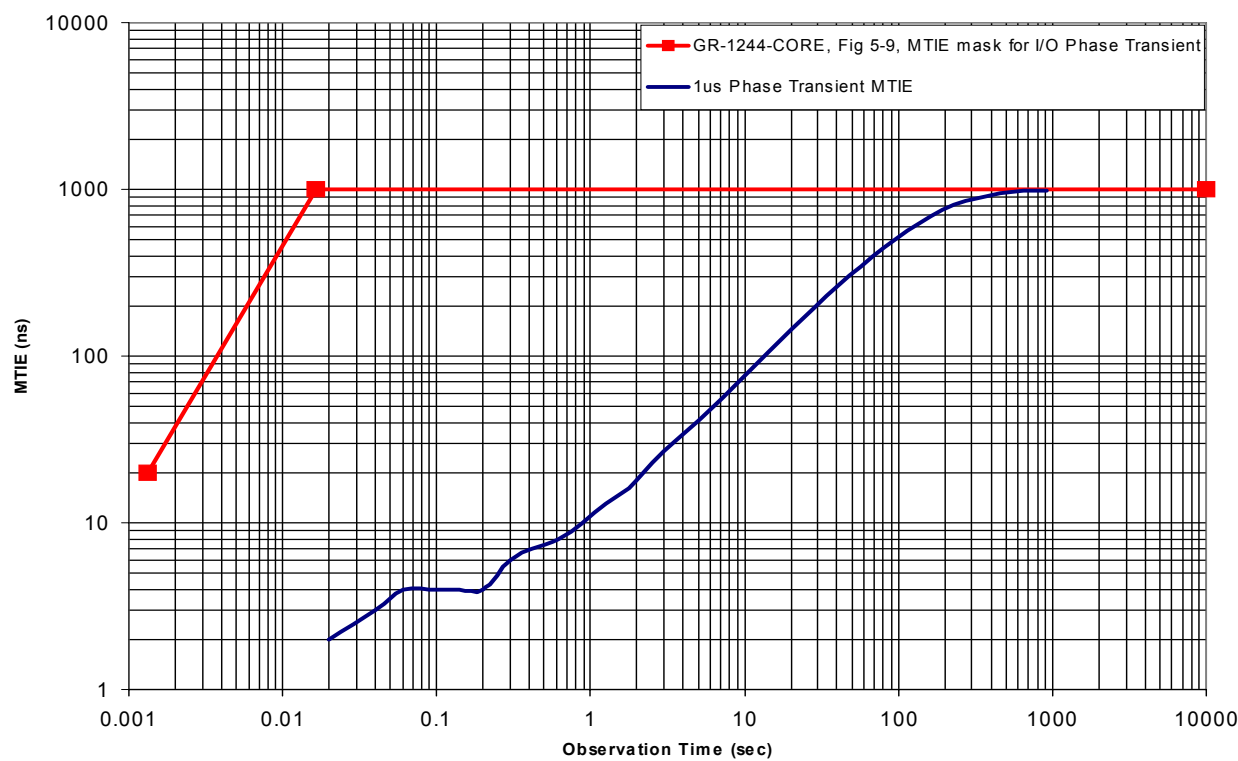
### 3E Entry into Hold Over MTIE

Figure 8



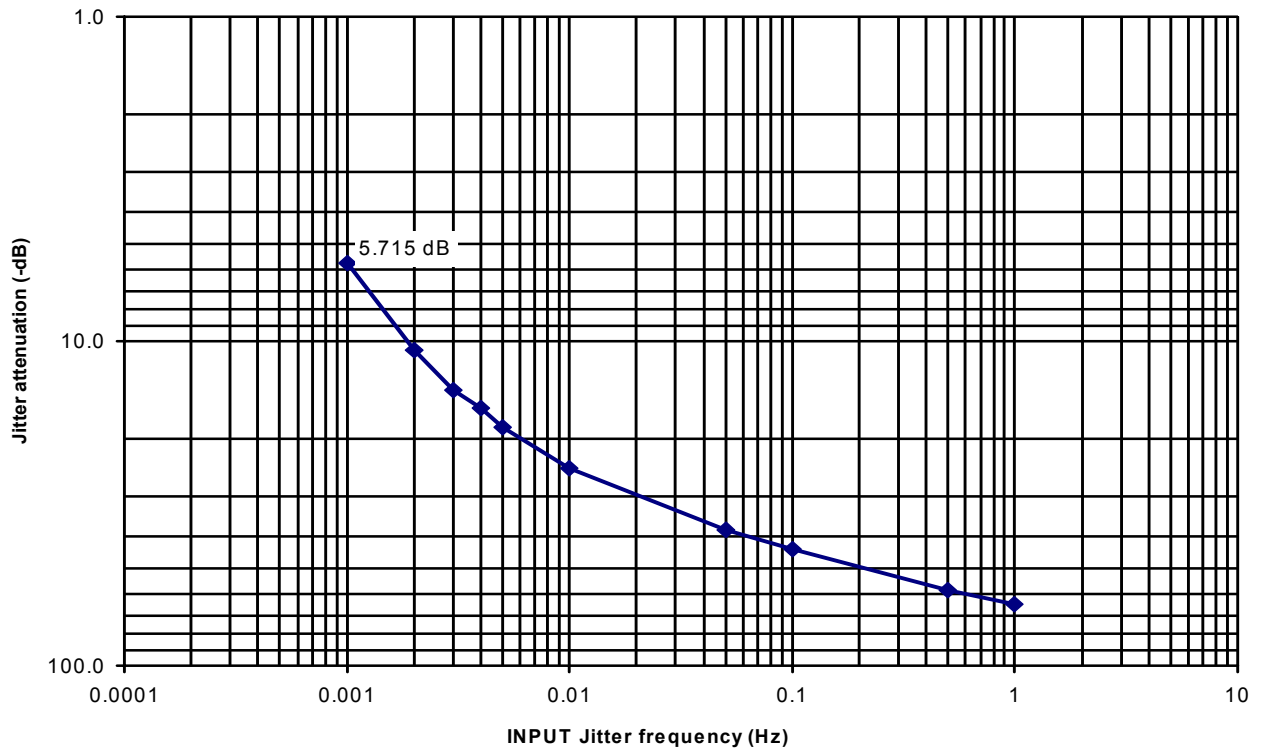
### 3E 1μs Phase Transient MTIE

Figure 9



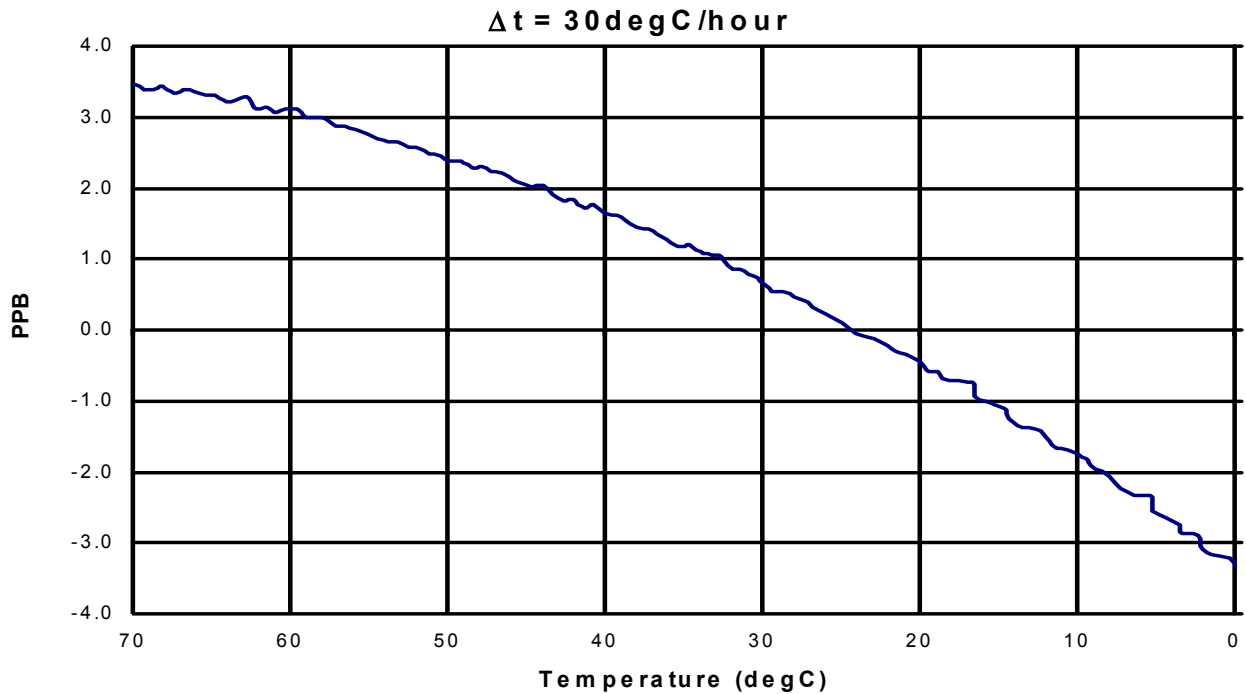
### 3E Jitter Attenuation

Figure 10



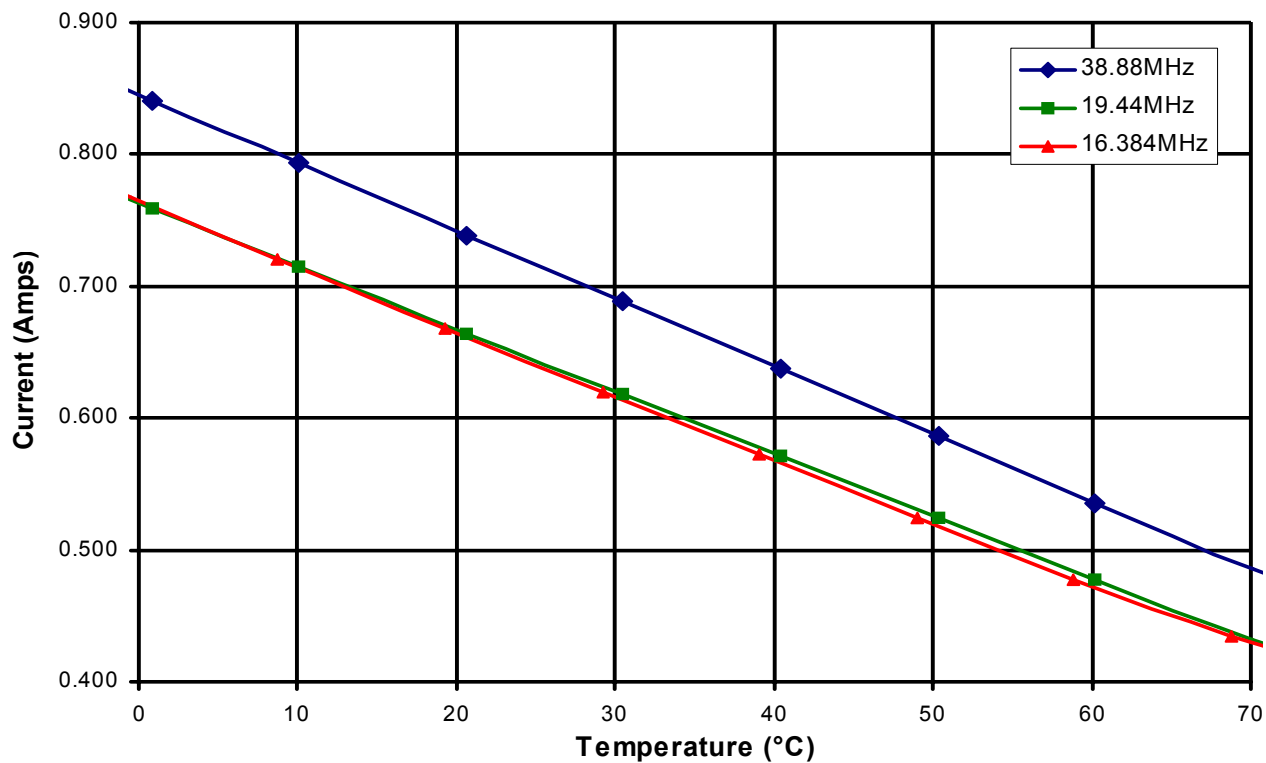
### Hold Over Stability over Temperature

Figure 11



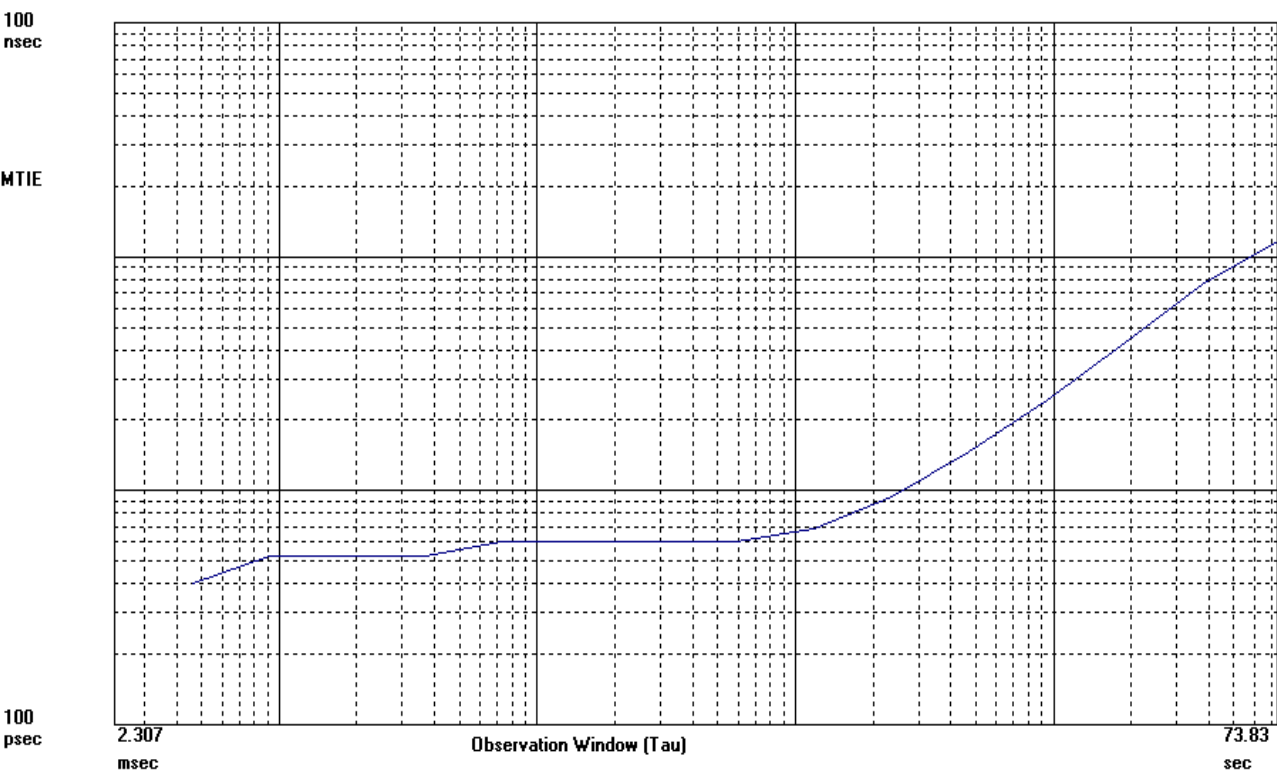
# Typical Current Consumption Over Temperature

Figure 12



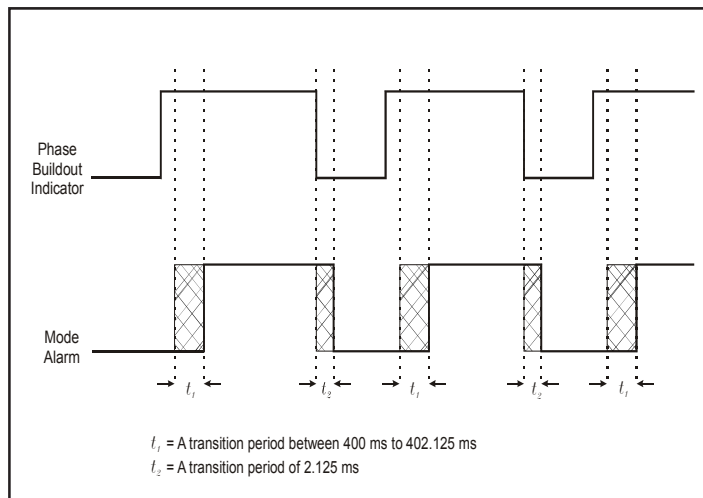
# 3E Typical Phase Build Out MTIE

Figure 13



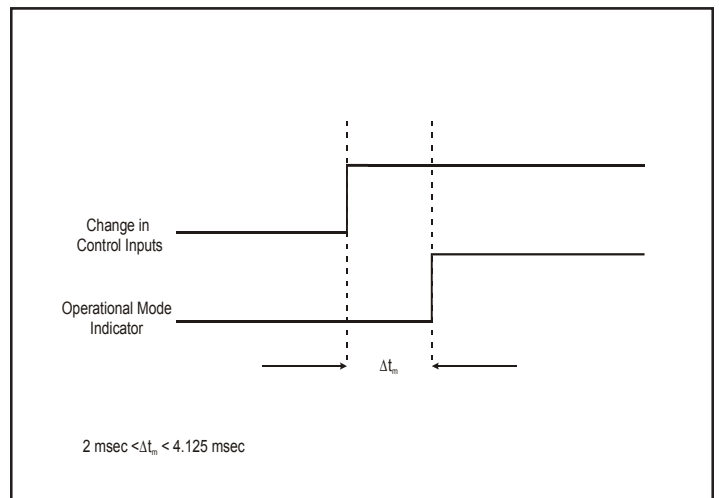
## 3E Phase Build Out $\geq 34$ ppm Frequency Change

Figure 14



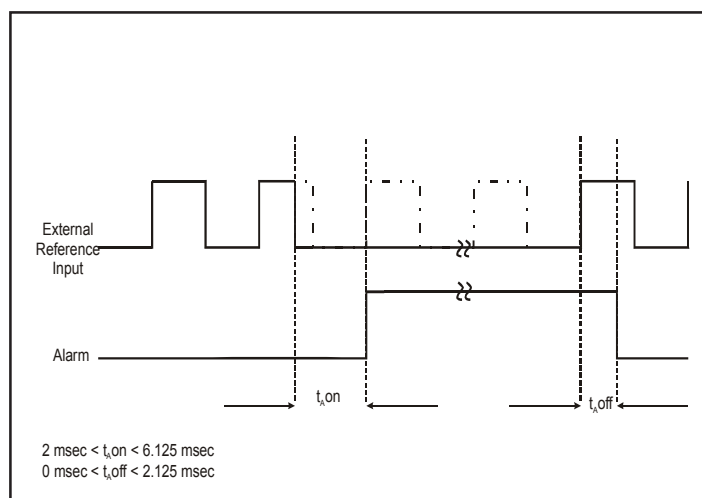
## Mode Switch Timing

Figure 15



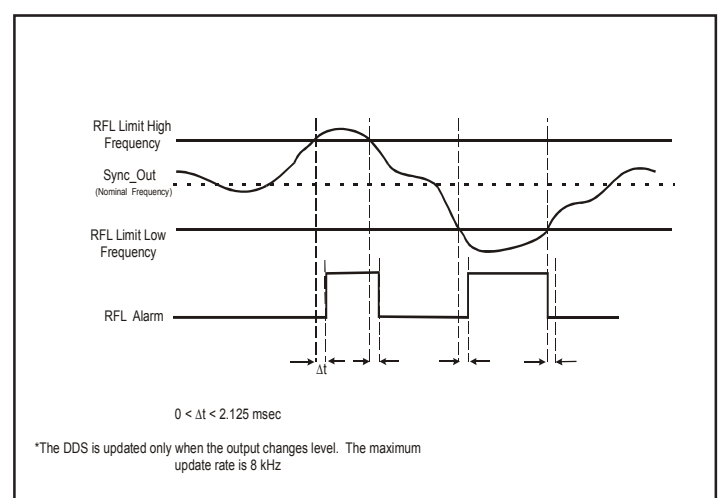
## Loss of Reference Timing

Figure 16



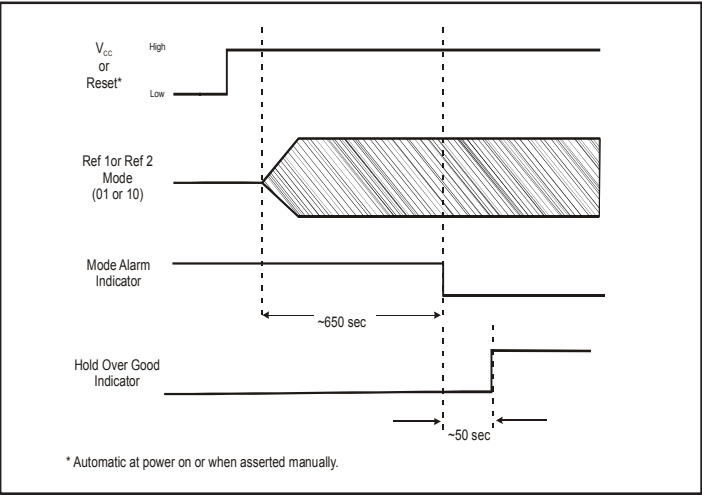
## RFL Alarm Timing

Figure 17



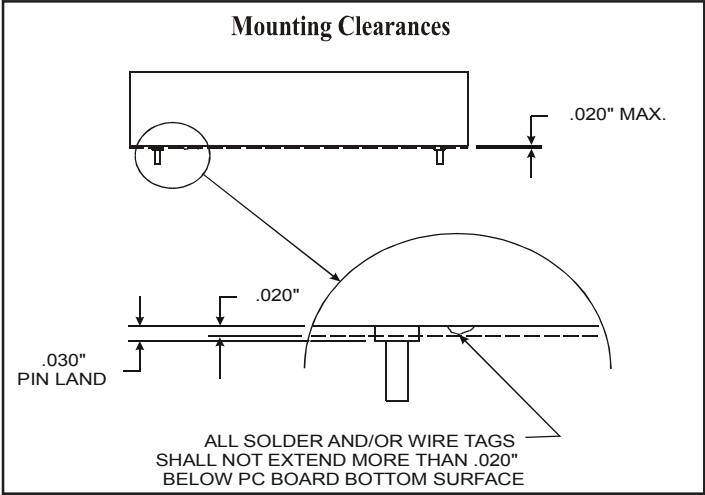
# Hold Over Good Timing

Figure 18



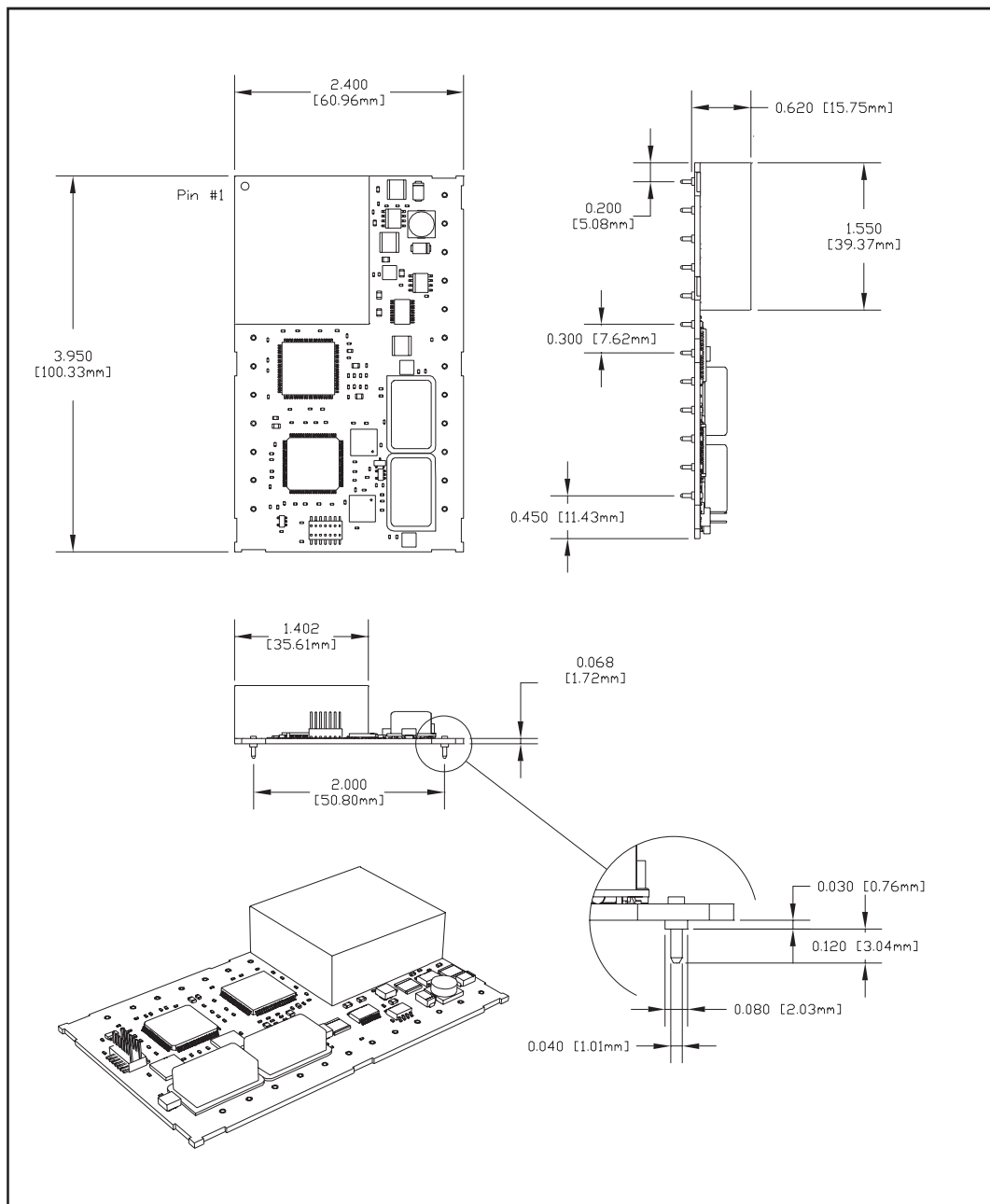
# Mounting Clearance Dimensions

Figure 19



## Package Dimensions

Figure 20





2111 Comprehensive Drive  
Aurora, Illinois 60505  
Phone: 630-851-4722  
Fax: 630-851-5040  
[www.conwin.com](http://www.conwin.com)

| Revision # | Revision Date | Notes                               |
|------------|---------------|-------------------------------------|
| P00        | 6/29/00       | Preliminary informational release   |
| P01        | 8/28/00       | Included additional frequencies     |
| P02        | 10/16/00      | Changed format                      |
| P03        | 6/6/01        | Changed to reflect new enhancements |
| P04        | 9/18/01       | Added 5V tolerant note              |
| P05        | 3/6/02        | Changed mech. height to 0.620       |
| P06        | 5/20/02       | Updated Fig.9                       |