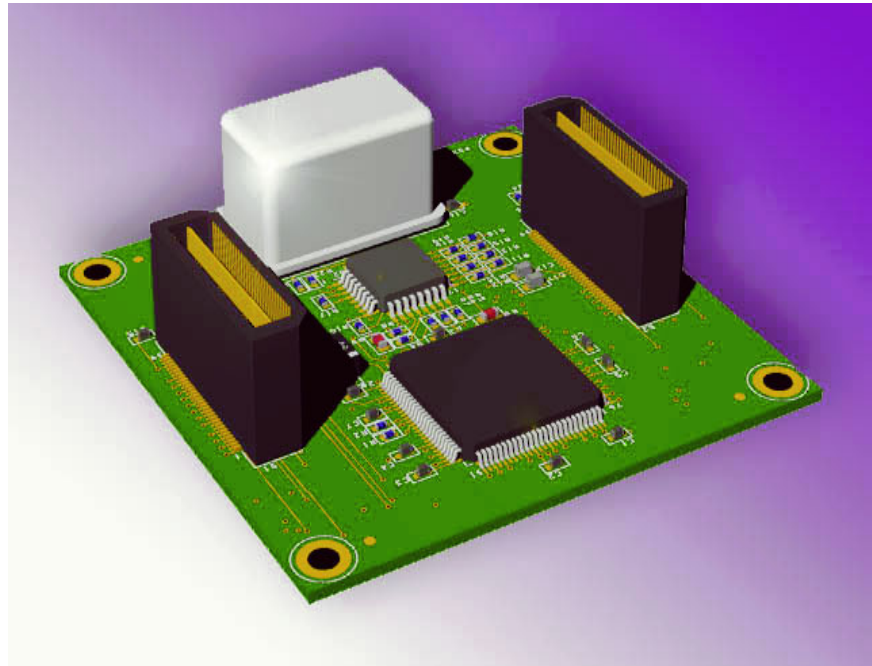


STS-101 Synchronous Timing Module

2111 Comprehensive Drive
Aurora, Illinois 60505
Phone: 630-851-4722
Fax: 630-851-5040
www.conwin.com



Features

- Suitable for Stratum 3 and 4 SONET or SDH Equipment Clocks (SEC) applications
- Supports six TTL/CMOS inputs and two BITS
- 8 differential (LVPECL) outputs
- Supports Free Run, Lock and Hold Over modes of operation.
- Robust monitoring on all input clock sources
- Automatic “hitless” switchover on loss of input.
- Phase build-out for output clock phase continuity during input switch over or mode transitions.
- Supports Microprocessor interface – Intel, Motorola, Multiplexed, Serial and EEPROM
- Programmable wander/jitter tracking/attenuation 0.1Hz to 20Hz
- Supports master/Slave configuration and hot/standby redundancy.
- 3.3V operation.
- Meets Telcordia specifications for Stratum 3 clocks.

Bulletin	TM028
Page	1 of 8
Revision	A02
Date	10 OCT 01
Issued By	MBatts

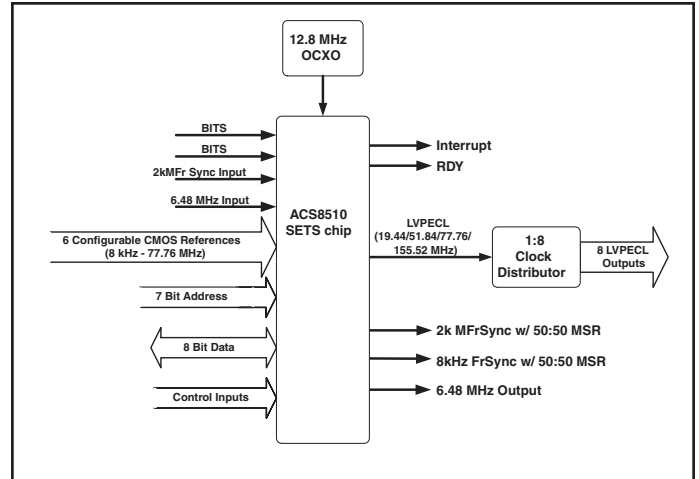
Application

The STS-101 module provides Synchronous Equipment Timing Source (SETS) function in a SONET/SDH network element. It generates SONET/SDH equipment clocks (SEC) and frame synchronization clocks. The module supports Free Run, Locked and Holdover modes of operations. The module supports six configurable CMOS input clocks and two BITS clocks and generates eight differential outputs (LVPECL). The module also supports master/slave configuration, which provides protection against single STS-101 failure. This module is incorporated with a microprocessor port, which provides access to the internal registers.

The STS-101 module is a platform that is designed to support easy installation and upgrade paths of the ACS8510 SETS chip from Semtech. For register assignments, please refer to the ACS8510 data sheet.

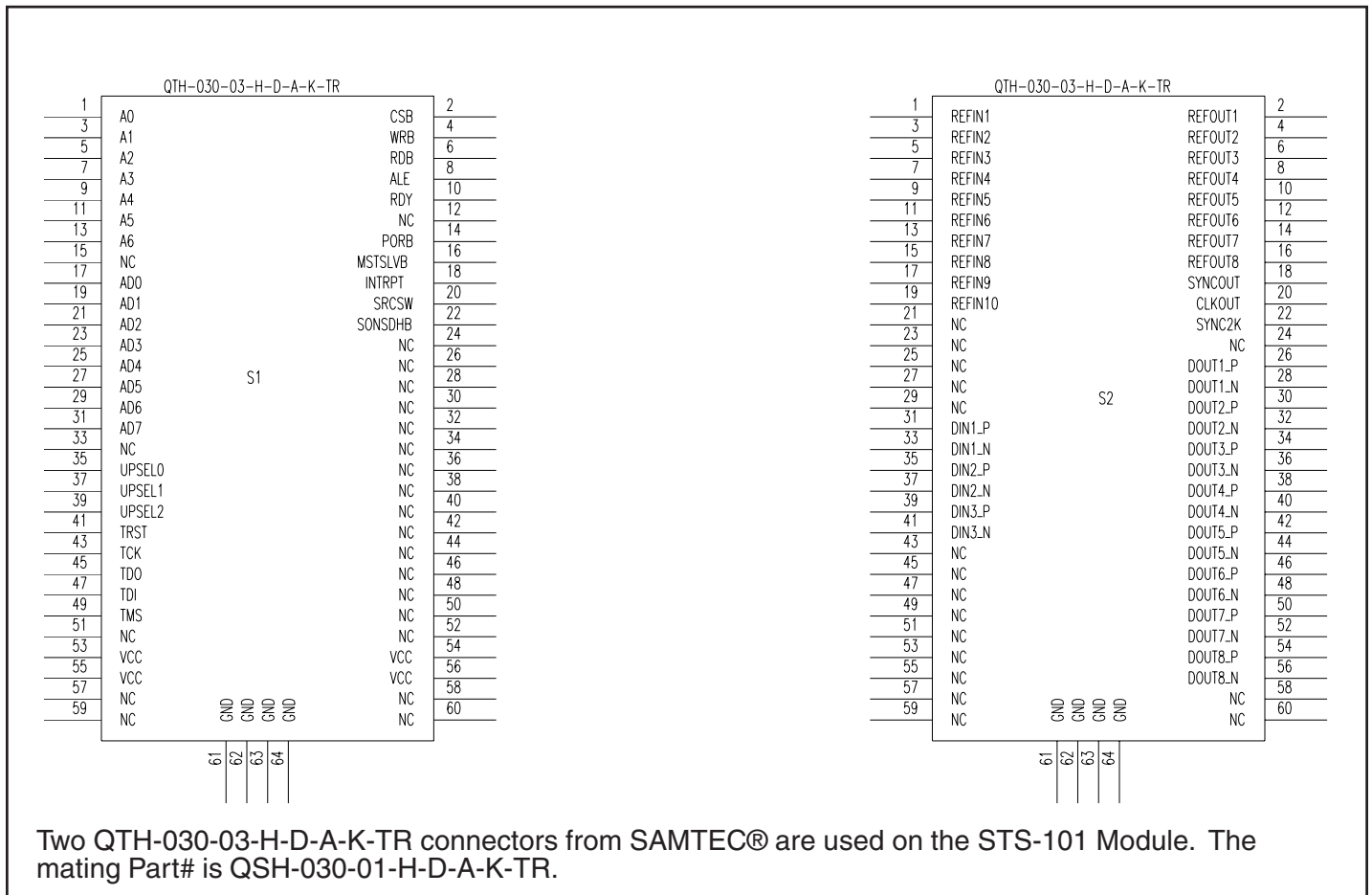
Functional Block Diagram

Figure 1



Pin Outs

Figure 2



Absolute Maximum Rating

Table 1

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
V_{CC}	Power Supply Voltage	-0.5		3.6	Volts	
V_I	Input Voltage			3.6	Volts	
V_O	Output Voltage			3.6	Volts	
T_s	Storage Temperature	-40		85	°C	

Recommended Operating Conditions

Table 2

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
V_{CC}	Power Supply Voltage	3.0	3.3	3.6	Volts	
I_{CC}	Power Supply Current		640	970	mA	
T_{OP}	Operating Temperature	0		70	°C	
V_{IH}	High level input voltage - TTL/CMOS	Refer to Semtech's data sheet for ACS8510 SETS				
V_{IL}	Low level input voltage - TTL/CMOS	Refer to Semtech's data sheet for ACS8510 SETS				
V_{IH}	High level input voltage - LVPECL	Refer to Semtech's data sheet for ACS8510 SETS				
V_{IL}	Low level input voltage - LVPECL	Refer to Semtech's data sheet for ACS8510 SETS				

DC Characteristics - Outputs

Table 3

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
V_{OH}	High level output voltage, TTL/CMOS	Refer to Semtech's data sheet for ACS8510 SETS				
V_{OL}	Low level output voltage, TTL/CMOS	Refer to Semtech's data sheet for ACS8510 SETS				
V_{OH}	High level output voltage, LVPECL	Refer to Semtech's data sheet for ACS8510 SETS				
V_{OL}	Low level output voltage, LVPECL	Refer to Semtech's data sheet for ACS8510 SETS				

Specifications

Table 4

Parameter	Specifications	Notes
Input Frequency Range	2kHz, 8kHz, 64kHz, 1.544MHz, 2.048MHz, 6.48MHz-77.76MHz	
Output Frequency Range	1.544MHz, 2.048MHz, 6.48MHz-155.52MHz	
Timing Reference Inputs	GR-1244-CORE 3.2.1	
Jitter, Wander and Phase Transient Tolerances	GR-1244-CORE 4.2-4.4, GR-253-CORE 5.4.4.3.6	
Wander Generation	GR-1244-CORE 5.3, GR-253-CORE 5.4.4.3.2	
Wander Transfer	GR-1244-CORE 5.4	
Jitter Generation	GR-1244-CORE 5.5, GR-253-CORE 5.6.2.3	
Jitter Transfer	GR-1244-CORE 5.5, GR-253-CORE 5.6.2.1	
Phase Transients	GR-1244-CORE 5.6, GR-253-CORE 5.4.4.3.3	
Free Run Accuracy	±4.6 ppm	
Pull-in/ Hold-in Range	±17 ppm from Free Run frequency	

Connector S1 Table 5

PIN	SYMBOL	I/O	DESCRIPTION
1,3,5,7, 9,11,13	A[0:6]	I	Address bus for microprocessor interface, A[0] is SDI in serial interface mode
2	CSB	I	Chip Select (Active Low)
4	WRB	I	Write (Active Low)
6	RDB	I	Read (Active Low)
8	ALE	I	Address latch enable. This pin acts as SCLK in serial mode.
10	RDY	O	Ready/Data acknowledge
14	PORB	I	Power on Reset (Active Low)
17,19,21 23,25,27 29,31	AD[0:7]		Address/Data multiplexed address/data depending on microprocessor mode selection. AD[0] is SDO in serial mode
16	MSTSLVB	I	Master/Slave select. Sets initial power up state
18	INTRPT	O	Active high software interrupt
20	SRCSW	I	Source switching. Force fast source switching.
22	SONSDHB	I	SONET/SDH frequency select. Sets initial power up state
35, 37, 39	UPSEL[0:2]	I	Configures the input for a particular microprocessor type.
41	TRST	I	Tri-State input
43	TCK	I	JTAG TCK input
45	TDO	O	JTAG TDO output
47	TDI	I	JTAG TDI input
49	TMS	I	JTAG TMS output
53, 54, 55, 56	Vcc		3.3V Input
61, 62, 63, 64	GND		Ground
12, 15, 24, 26, 28, 30, 32, 33, 34, 36, 38, 40, 42, 44, 46, 48, 50, 51, 52, 57, 58, 59, 60	NC		No Connect

Connector S2 Table 6

PIN	SYMBOL	I/O	IO Type	DESCRIPTION
1	REFIN1	I	TTL/CMOS	Input Reference @ 8kHz (I3 input on ACS8510 SETS)
2	REFOUT1	O	TTL/CMOS	Output clock @ 6.48 MHz (TO1 output on ACS8510 SETS)
3	REFIN2	I	TTL/CMOS	Input Reference @ 8kHz (I4 input on ACS8510 SETS)
4	REFOUT2	O	TTL/CMOS	No Connect
5	REFIN3	I	TTL/CMOS	Input Reference @ 8kHz (I7 input on ACS8510 SETS)
6	REFOUT3	O	TTL/CMOS	No Connect
7	REFIN4	I	TTL/CMOS	Input Reference @ 8kHz (I8 input on ACS8510 SETS)
8	REFOUT4	O	TTL/CMOS	No Connect
9	REFIN5	I	TTL/CMOS	Input Reference @ 8kHz (I9 input on ACS8510 SETS)
10	REFOUT5	O	TTL/CMOS	No Connect
11	REFIN6	I	TTL/CMOS	Input Reference @ 8kHz (I10 input on ACS8510 SETS)

Connector S2 Table 6 (Continued)

12	REFOUT6	O	TTL/CMOS	No Connect
13	REFIN7	I	TTL/CMOS	Input Reference @ 6.48MHz (For slave operation)
14	REFOUT7	O	TTL/CMOS	8 kHz Frame SYNC output
15	REFIN8	I	TTL/CMOS	BITS input
16	REFOUT8	O	TTL/CMOS	2 kHz Multi-Frame SYNC output
17	REFIN9	I	TTL/CMOS	BITS input
18	SYNCOUT	O	TTL/CMOS	No Connect
19	REFIN10	I	TTL/CMOS	No Connect
20	CLKOUT	O	TTL/CMOS	Onboard oscillator output
22	SYNC2K	I	TTL/CMOS	Synchronized to a 2 kHz multi-frame signal from partner STS-100A in a redundancy system
26	DOUT1_P	O	LVPECL	LVPECL Output
28	DOUT1_N	O	LVPECL	LVPECL Output
30	DOUT2_P	O	LVPECL	LVPECL Output
32	DOUT2_N	O	LVPECL	LVPECL Output
34	DOUT3_P	O	LVPECL	LVPECL Output
36	DOUT3_N	O	LVPECL	LVPECL Output
38	DOUT4_P	O	LVPECL	LVPECL Output
40	DOUT4_N	O	LVPECL	LVPECL Output
42	DOUT5_P	O	LVPECL	LVPECL Output
44	DOUT5_N	O	LVPECL	LVPECL Output
46	DOUT6_P	O	LVPECL	LVPECL Output
48	DOUT6_N	O	LVPECL	LVPECL Output
50	DOUT7_P	O	LVPECL	LVPECL Output
52	DOUT7_N	O	LVPECL	LVPECL Output
54	DOUT8_P	O	LVPECL	LVPECL Output
56	DOUT8_N	O	LVPECL	LVPECL Output
31	DIN1_P	I	No Connect	
33	DIN1_N	I	No Connect	
35	DIN2_P	I	No Connect	
37	DIN2_N	I	No Connect	
39	DIN3_P	I	No Connect	
41	DIN3_N	I	No Connect	
21,23,25,27, 29,43,45, 47, 49,51,53,55, 57,58,59,60	NC			No Connect
61,62,63,64	GND		Ground	

Microprocessor Interface

The STS-101 has a microprocessor interface incorporated into the module. The module can be configured to function in the modes listed in Table 7. The module is configured by using pins UPSEL[2:0].

Table 7

UPSEL[2:0]	MODE
000	Off
001	EEPROM
010	Multiplexed
011	INTEL
100	MOTOROLA
101	Serial
110	Off
111	Off

MOTOROLA mode: Parallel data + address. Compatible with 68x0 type bus.

INTEL mode: Parallel data + address. Compatible with 80x86 type bus.

Multiplexed mode: Data/address. Mode is suitable for microprocessors, which share bus signals between data and address.

Serial mode: Compatible with serial interface.

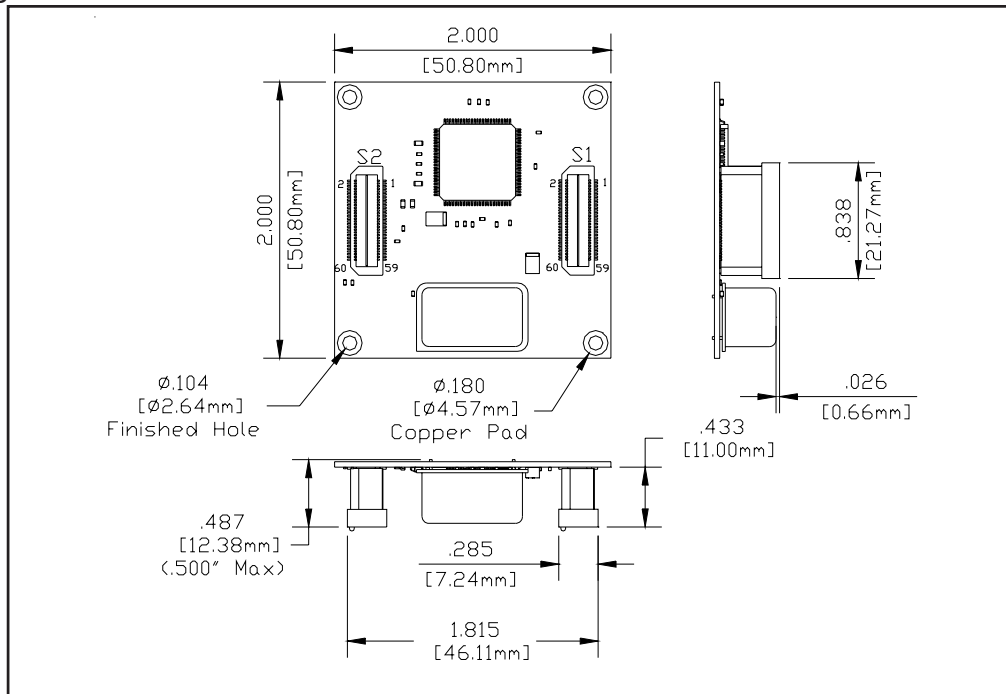
EEPROM mode: This mode is suitable for use with an EEPROM, in which configuration information is stored (one way communication- status information not accessible).

--For timing diagrams, please refer to ACS8510 data sheet.

Package Dimensions

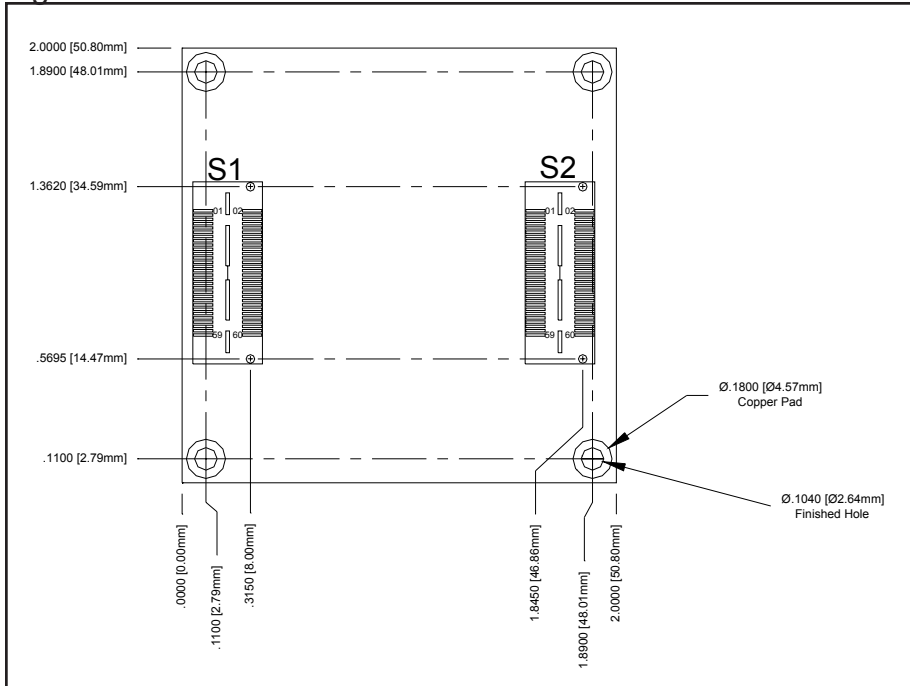
Maximum Board Dimension: L x W x H = 2" x 2" x 0.5"

Fig 3



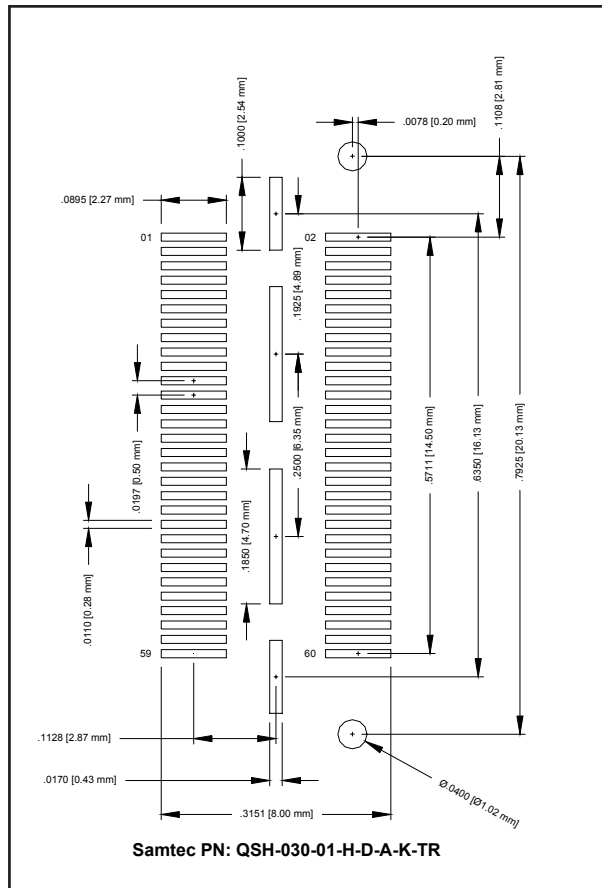
Recommended Connector Placement and Component Keep Out Area

Fig 4



Recommended Connector Footprint Dimensions

Fig 5



CONNOR WINFIELD



2111 Comprehensive Drive
Aurora, Illinois 60505
Phone: 630-851-4722
Fax: 630-851-5040
www.conwin.com

Revision	Revision Date	Note
A00	7/30/01	Advance Information
A01	11/26/01	Updated to reflect design changes
A02	10/10/02	Added millimeter to mechanical drawings
