STC5130
Synchronous Clock for SETS
Data Sheet

Description

The STC5130 is an integrated single chip solution for the synchronous clock in SDH, SONET, and Synchronous Ethernet network elements. The device is fully compliant with ITU-T G.813, and Telcordia GR1244, and GR253.

The STC5130 accepts 12 reference inputs and generates 8 independent synchronized output clocks. Reference input frequencies are automatically detected, and inputs are individually monitored for quality. Active reference selection may be manual or automatic. All reference switches are hitless. Synchronized outputs may be programmed for a wide variety of SONET and SDH as well as Synchronous Ethernet frequencies.

Two independent clock generators provide the standardized T0 and T4 functions. Each clock generator includes a DPLL (Digital Phase-Locked Loop), which may operate in the Freerun, Synchronized, and Holdover modes. Both clock generators support master/slave operation for redundant applications. The proprietary **SyncLink™** cross-couple data link provides master/slave phase information and state data to ensure seamless side switches.

A standard SPI serial bus interface or parallel bus provide access to the STC5130's comprehensive, yet simple to use internal control and status registers. The device operates with an external OCXO or TCXO as its MCLK at 20 MHz.

Features

- For SDH SETS
- For SONET Stratum 3, 4E, 4 and SMC, and Synchronous Ethernet
- Complies with ITU-T G.813, Telcordia GR1244, and GR253
- Supports Master/Slave operation with the **SyncLink™** cross-couple data link for master/slave redundant applications
- Accepts 12 individual clock reference inputs
- Reference clock inputs are automatically frequency detected
- Supports manual or automatic reference selection
- T0 and T4 have independent reference lists and priority tables for automatic reference selection
- 8 synchronized output clocks
- Output/input phase skew is adjustable in slave mode, in 0.1ns steps up to 200ns
- Hit-less reference and master/slave switching
- Phase rebuild on re-lock and reference switches
- Better than 0.1 ppb holdover accuracy
- Programmable bandwidth, from 90mHz to 107Hz, for both T0 and T4 DPLL
- Supports SPI or parallel bus interface
- IEEE 1149.1 JTAG boundary scan
- Available in TQFP100 package

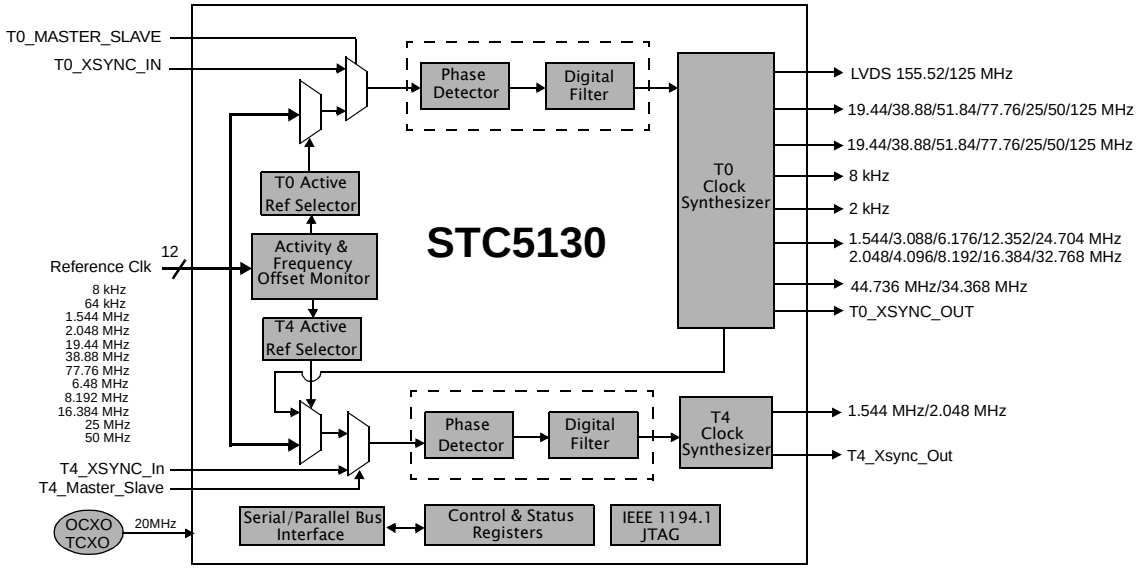

Figure 1: Functional Block Diagram

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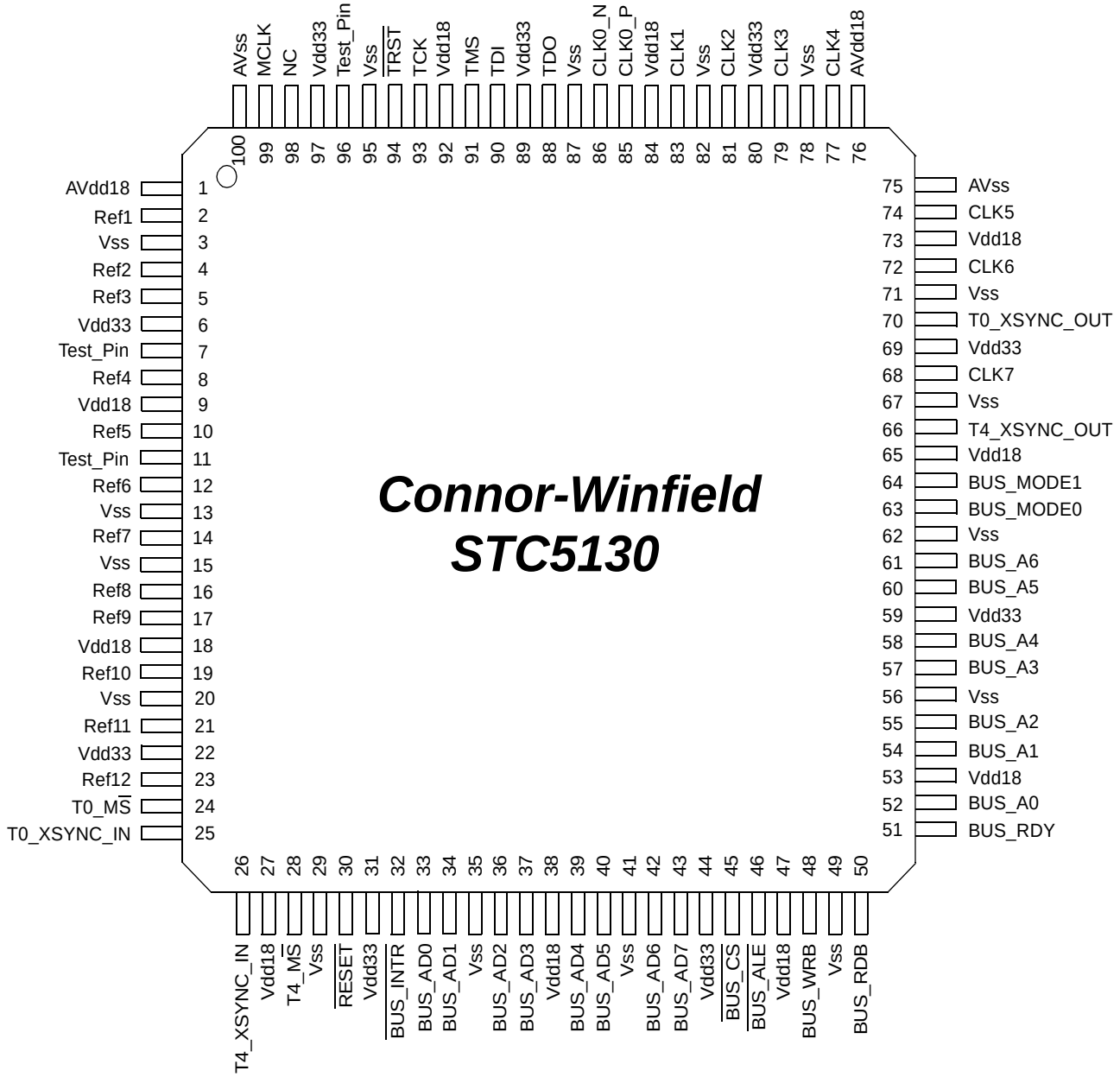
STC5130 Pin Diagram (Top View)



Note: Pins labeled “Test Pin” must be grounded.

STC5130 Pin Description

All I/O is LVCMOS, except for CLK0, which is LVDS.

Table 1: Pin Description

Pin Name	Pin #	I/O	Description
Vdd33	6,22,31, 44,59, 69,80, 89,97		3.3V power input
Vdd18	9,18,27, 38,47,53, 65,73,84, 92		1.8V power input
Vss	3,13,15, 20,29,35, 41,49,56, 62,67,71, 78,82,87, 95		Digital ground
AVdd18	1, 76		1.8V analog power input
AVss	75, 100		Analog ground
$\overline{\text{TRST}}$	94	I	JTAG boundary scan reset, active low
TCK	93	I	JTAG boundary scan clock
TMS	91	I	JTAG boundary scan mode selection
TDI	90	I	JTAG boundary scan data input
TDO	88	O	JTAG boundary scan data output
$\overline{\text{RESET}}$	30	I	Active low to reset the chip
MCLK	99	I	Master clock input, 20 MHz
BUS_MODE0	63	I	Bus mode selection, 00: SPI, 01: Motorola, 10: Intel, 11: Multiplex
BUS_MODE1	64	I	Bus mode selection, 00: SPI, 01: Motorola, 10: Intel, 11: Multiplex
$\overline{\text{BUS\_CS}}$	45	I	Parallel bus or SPI chip select ($\overline{\text{CS}}$)
$\overline{\text{BUS\_ALE}}$	46	I	Parallel bus address latch or SPI clock input (SCLK)
BUS_WRB	48	I	Parallel bus write
BUS_RDB	50	I	Parallel bus read or read/write input, or SPI data input (SDI)
BUS_RDY	51	O	Parallel bus ready output or SPI data output (SDO)
BUS_A6	61	I	Bus Address bit 6
BUS_A5	60	I	Bus Address bit 5
BUS_A4	58	I	Bus Address bit 4
BUS_A3	57	I	Bus Address bit 3
BUS_A2	55	I	Bus Address bit 2
BUS_A1	54	I	Bus Address bit 1
BUS_A0	52	I	Bus Address bit 0

Table 1: Pin Description

Pin Name	Pin #	I/O	Description
BUS_AD7	43	I/O	Parallel bus address/data bit7
BUS_AD6	42	I/O	Parallel bus address/data bit6
BUS_AD5	40	I/O	Parallel bus address/data bit5
BUS_AD4	39	I/O	Parallel bus address/data bit4
BUS_AD3	37	I/O	Parallel bus address/data bit3
BUS_AD2	36	I/O	Parallel bus address/data bit2
BUS_AD1	34	I/O	Parallel bus address/data bit1
BUS_AD0	33	I/O	Parallel bus address/data bit0
$\overline{\text{BUS\_INTR}}$	32	O	Interrupt
REF1	2	I	Reference input 1
REF2	4	I	Reference input 2
REF3	5	I	Reference input 3
REF4	8	I	Reference input 4
REF5	10	I	Reference input 5
REF6	12	I	Reference input 6
REF7	14	I	Reference input 7
REF8	16	I	Reference input 8
REF9	17	I	Reference input 9
REF10	19	I	Reference input 10
REF11	21	I	Reference input 11
REF12	23	I	Reference input 12
T0_M/$\overline{\text{S}}$	24	I	Select master or slave mode for T0, 1: Master, 0: Slave
T4_M/$\overline{\text{S}}$	28	I	Select master or slave mode for T4, 1: Master, 0: Slave
T0_XSYNC_IN	25	I	Cross-couple **SyncLink™** data link input for T0 for master/slave redundant applications
T0_XSYNC_OUT	70	O	Cross-couple **SyncLink™** data link output for T0 for master/slave redundant applications
T4_XSYNC_IN	26	I	8kHz cross-couple link input for T4 for master/slave redundant applications
T4_XSYNC_OUT	66	O	8kHz cross-couple link output for T4 for master/slave redundant applications
CLK0_P	85	O[1]	155.52/125 MHz LVDS output (T0)
CLK0_N	86	O[1]	155.52/125 MHz LVDS output (T0)
CLK1	83	O	19.44/38.88/51.84/77.76/25/50/125 MHz (T0)
CLK2	81	O	19.44/38.88/51.84/77.76/25/50/125 MHz (T0)
CLK3	79	O	8 kHz frame pulse or 50% duty cycle clock (T0)
CLK4	77	O	2 kHz frame pulse or 50% duty cycle clock (T0)
CLK5	74	O	44.736/34.368 MHz (T0)
CLK6	72	O	1.544/3.088/6.176/12.352/24.704/2.048/4.098/8.192/16.384/32.768 MHz (T0)
CLK7	68	O	1.544/2.048 MHz (T4)

Table 1: Pin Description

Pin Name	Pin #	I/O	Description
NC	98		No connection. Pin can be left open, floating, tied up, or grounded.
Test_Pin	7,11,96	I	Test pin, must be grounded for normal operation

Note 1: All I/O is LVCMOS, except for CLK0, which is LVDS

Absolute Maximum Ratings

Table 2: Absolute Maximum Ratings

Symbol	Parameter	Min.	Max	Units	Notes
Vdd33	Logic power supply voltage, 3.3V	-0.5	4.5	volts	2
Vdd18	Logic power supply voltage, 1.8V	-0.5	2.5	volts	2
AVdd18	Analog power supply voltage, 1.8V	-0.5	2.5	volts	2
VIN	Logic input voltage	-0.5	5.5	volts	2
TSTG	Storage Temperature	-65	150	°C	2

Note 2: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the Recommended Operating Conditions.

Operating Conditions and Electrical Characteristics

Table 3: Recommended Operating Conditions and Electrical Characteristics

Symbol	Parameter	Min.	Nominal	Max.	Units	Notes
Vdd33	3.3V digital power supply voltage	3.0	3.3	3.6	Volts	
Vdd18	1.8V digital power supply voltage	1.65	1.8	1.95	Volts	
AVdd18	1.8V analog power supply voltage	1.65	1.8	1.95	Volts	
CIN	Input capacitance		8		pF	
TRIP	Input reference signal positive pulse width	10			ns	
TRIN	Input reference signal negative pulse width	10			ns	
TA	Operating Ambient Temperature Range (Commercial)	0		70	°C	
TA	Operating Ambient Temperature Range (Industrial)	-40		85	°C	
Icc (Vcc)	3.3V digital supply current		TBD		mA	
Icc (AVcc)	3.3V analog supply current		TBD		mA	
Pd	Device power dissipation		TBD		W	

Table 3: Recommended Operating Conditions and Electrical Characteristics

Symbol		Parameter	Min.	Nominal	Max.	Units	Notes
VIH (3.3V)	LVCMOS	High level input voltage	2.0		5.5	Volts	3
VIL (3.3V)		Low level input voltage	-0.3		0.8	Volts	3
VOH (3.3V)		High level output voltage (IOH = -12mA)	2.4			Volts	3
VOL (3.3V)		Low level output voltage (IOL =12mA)			0.4	Volts	3
V_T		Threshold point	1.45	1.58	1.74	Volts	3
I_L		Input Leakage Current	-10		10	uA	3
Voh	LVDS	Output voltage high			1475	mV	
Vol		Output voltage low	925			mV	
Vod		Output differential voltage	250		450	mV	
Vos		Output offset voltage	1125		1375	mV	
ΔVod		Change in Vod between “0” and “1”			50 / 150	mV	4
ΔVos		Change in Vos between “0” and “1”			50	mV	
Isa, Isb		Output current - driver shorted to ground			24	mA	
Isab		Output current - drivers shorted together			12	mA	

Note 3: LVCMOS 3.3 compatible
Note 4: ‘50mV’ for steady state and ‘150mV’ for dynamic

Register Map

Table 4: Register Map

Addr	Reg Name	Bits	Type	Description
0x00	Chip_ID	15-0	R	Chip ID, 0x5130
0x02	Chip_Rev	7-0	R	Chip revision number
0x03	Chip_Sub_Rev	7-0	R	Chip sub-revision
0x04	T0_T4_MS_Sts	1-0	R	Indicates master/slave state
0x05	T0_Slave_Phase_Adj	11-0	R/W	Adjust T0 slave phase from 0 ~ 409.5 ns in 0.1 ns steps
0x07	T4_Slave_Phase_Adj	11-0	R/W	Adjust T4 slave phase from 0 ~ 409.5 ns in 0.1 ns steps
0x09	Fill_Obs_Window	3-0	R/W	Leaky bucket fill observation window, 1 ~ 16 ms
0x0a	Leak_Obs_Window	3-0	R/W	Leaky bucket leak observation window, 1 ~ 16 times the Fill_Obs_Window
0x0b	Bucket_Size	5-0	R/W	Leaky bucket size, 1 ~ 63
0x0c	Assert_Threshold	5-0	R/W	Leaky bucket alarm assert threshold, 1 ~ 63
0x0d	De_Assert_Threshold	5-0	R/W	Leaky bucket alarm de-assert threshold, 0 ~ 62
0x0e	Freerun_Cal	10-0	R/W	Freerun calibration, - 102.4 ~ + 102.3 ppm
0x10	Disqualification_Range	9-0	R/W	Reference disqualification range (pull-in range), 0 ~ 102.3 ppm
0x12	Qualification_Range	9-0	R/W	Reference qualification range, 0 ~ 102.3 ppm
0x14	Qualification_Timer	5-0	R/W	Reference qualification timer, 0 ~ 63 s
0x15	Ref_Selector	3-0	R/W	Determines which reference data is shown in register 0x16
0x16	Ref_Frq_Offset	15-0	R	Reference frequency and frequency offset of the reference selected by register 0x15
0x18	Refs_Activity	13-0	R	Reference and cross reference activity
0x1a	Refs_Qual	11-0	R	Reference 1 ~ 12 qualification
0x1c	T0_Control_Mode	5-0	R/W	OOP -Follow/Don't Follow, Manual/Auto, Revertive, HO_Usage, PhaseAlignMode
0x1d	T0_Bandwidth	4-0	R/W	Loop bandwidth selection
0x1e	T0_Auto_Active_Ref	3-0	R	Indicates automatically selected reference
0x1f	T0_Manual_Active_Ref	3-0	R/W	Selects the active reference in manual mode
0x20	T0_Device_Holdover_History	31-0	R	Device Holdover History for T0 relative to MCLK
0x24	T0_Long_Term_Accu_History	31-0	R	Long term Accumulated History for T0 relative to MCLK
0x28	T0_Short_Term_Accu_History	31-0	R	Short term Accumulated History for T0 relative to MCLK
0x2c	T0_User_Accu_History	31-0	R/W	User Holdover data for T0 relative to MCLK
0x30	T0_History_Ramp	6-0	R/W	Bits 6-4, Long term history accumulation bandwidth: 9.7, 4.9, 2.4, 1.2, 0.61, 0.03 mHz Bits3-2, Short term history accumulation bandwidth: 2.5, 1.24, 0.62, 0.31 Hz Bits 1-0, Ramp control: none, 1, 1.5, 2 ppm/s
0x31	T0_Priority_Table	47-0	R/W	REF1-12 selection priority for automatic mode, 4 bits/reference
0x37	T0_PLL_Status	7-0	R	OOP, LOL, LOS, Sync, HHA, AHR, SAP
0x38	T0_Accu_Flush	0-0	W	0: Flush/reset the long-term history, 1: Flush/reset both the long-term and the device holdover history
0x39	T4_Control_Mode	5-0	R/W	OOP -Follow/Don't Follow, Manual/Auto, Revertive, HO_Usage, PhaseAlignMode
0x3a	T4_Bandwidth	4-0	R/W	Loop bandwidth selection
0x3b	T4_Auto_Active_Ref	3-0	R	Indicates automatically selected reference
0x3c	T4_Manual_Active_Ref	3-0	R/W	Selects the active reference in manual mode
0x3d	T4_Device_Holdover_History	31-0	R	Device Holdover History for T4 relative to MCLK

Table 4: Register Map

Addr	Reg Name	Bits	Type	Description
0x41	T4_Long_Term_Accu_History	31-0	R	Long term Accumulated History for T4 relative to MCLK
0x45	T4_Short_Term_Accu_History	31-0	R	Short term Accumulated History for T4 relative to MCLK
0x49	T4_User_Accu_History	31-0	R/W	User Holdover data for T4 relative to MCLK
0x4d	T4_History_Ramp	6-0	R/W	Bits 6-4, Long term history accumulation bandwidth: 9.7, 4.9, 2.4, 1.2, 0.61, 0.03 mHz Bits3-2, Short term history accumulation bandwidth: 2.5, 1.24, 0.62, 0.31 Hz Bits 1-0, Ramp control: none, 1, 1.5, 2 ppm/s
0x4e	T4_Priority_Table	47-0	R/W	REF1-12 selection priority for automatic mode, 4 bits/reference
0x54	T4_PLL_Status	7-0	R	OOP, LOL, LOS, Sync, HHR, AHR, SAP
0x55	T4_Accu_Flush	0-0	W	0: Flush/reset the long-term history, 1: Flush/reset both the long-term and the device holdover history
0x56	CLK0_Sel	1-0	R/W	155.52/125 MHz clock select or disable for CLK0
0x57	CLK1_Sel	2-0	R/W	19.44/38.88/51.84/77.76/25/50/125 MHz or disable select for CLK1
0x58	CLK2_Sel	2-0	R/W	19.44/38.88/51.84/77.76/25/50/125 MHz or disable select for CLK2
0x59	CLK3_Sel	5-0	R/W	8kHz output 50% duty cycle or pulse width selection for CLK3
0x5a	CLK4_Sel	5-0	R/W	2kHz output 50% duty cycle or pulse width selection for CLK4
0x5b	CLK5_Sel	1-0	R/W	DS3/E3 select for CLK5
0x5c	CLK6_Sel	3-0	R/W	DS1 x n / E1 x n selector for CLK6
0x5d	CLK7_Sel	1-0	R/W	DS1/E1 selector for CLK7
0x5e	Intr_Event	9-0	R/W	Interrupt event
0x60	Intr_Enable	9-0	R/W	Interrupt enable

General Description

The STC5130 is an integrated single chip solution for the synchronous clock in SDH (SETS), SONET, and Synchronous Ethernet network elements. Its highly integrated design implements all of the necessary reference selection, monitoring, digital filtering, synthesis, and control functions. An external OCXO or TCXO at 20 MHz completes a system level solution (see Functional Block Diagram, Figure 1).

The STC5130 includes two independent DPLLs (Digital Phase-Locked Loop) implementing the timing functions of T0 and T4. Each may select one of 12 reference inputs as its active reference. In addition, T4 may select T0's output as it's reference. T0 provides 7 of the chip's 8 clock outputs while T4 provides one clock output. Additionally, both T0 and T4 provide a cross reference output for master/slave applications.

Reference frequencies are autodetected and may each be 8kHz, 64kHz, 1.544MHz, 2.048MHz, 19.44MHz, 38.88MHz, 77.76MHz, 6.48MHz, 8.192MHz, 16.384MHz, 25MHz, or 50MHz. Each reference input is continuously monitored for activity and frequency offset. Activity monitoring is implemented with a leaky bucket accumulator with programmable fill and leak rates. Frequency offset is determined relative to the freerun clock, which is digitally calibrated from MCLK (the external TCXO/OCXO). A reference is desiganted as "qualified" if it is active and its frequency is within the programmed frequency offset range for a pre-programmed time.

Active references may be selected manually or automatically, individually selectable for T0 and T4. In manual mode, the active reference is selected under application control, independant of it's qualification status.

In automatic mode, the active reference is selected according to revertivity status, and each reference's priority and qualification. Reference priorities are individually programmable. T0 and T4 each have their own priority tables. While a current active reference is qualified, revertivity determines whether a higher priority qualified reference should preempt the current active reference.

The two independent clock generators, T0 and T4, each includes a DPLL, which may operate in the Freerun, Synchronized, and Holdover modes. Both clock generators support master/slave operation for redundant applications. T0 generates the proprietary **SyncLink^{TM}** cross-couple data link, which provides master/slave phase information and state data to ensure seamless side switches. T4 provides an 8kHz cross-couple signal. The slave output clock phase is user adjustable.

The T0 and T4 clock generators may each be in freerun, synchronized, or holdover modes. In freerun, the clock outputs are synthesized and digitally calibrated from the MCLK. The stability of freerun is simply determined by the external OCXO/TCXO. In synchronized mode, the chip phase locks to the selected input reference. Phase lock may be selected as arbitrary or zero phase offset between the reference and clock outputs. All reference switches are performed in a hitless manner, and frequency ramp controls ensure smooth output signal transitions. When references are switched, the device will minimize phase transitions in the output clocks. While synchronized, a frequency history is accumulated. In holdover mode, the chip outputs are synthesized according to this or a user supplied history.

The Digital Phase Locked Loop which provides the critical filtering and frequency/phase control functions is implemented with the NOVA kernel - a set of well-proven algorithms and control that meet or exceed all requirements and lead the industry in critical jitter and accuracy performance parameters. Loop bandwidth may be user configured.

The device generates 8 independent synchronized output clocks. The first is at 155.52/125MHz. The second and third clocks may be programmed at 6.48/19.44/38.88/51.84/77.76/25/50/125MHz. The fourth and fifth are at 8kHz and 2kHz. The sixth is programmable at 1, 2, 4, 8, or 16 x T1 or E1 rate. The seventh is programmable at either DS3 or E3 rate. The eigth (generated by T4) is programmable at either T1 or E1 rate.

Control functions are provided either via a standard SPI serial bus interface or 8-bit parallel bus interface. These provide access to the STC5130's comprehensive, yet simple to use internal control and status registers. Parallel bus operation is supported in the Motorola mode, Intel mode, or Multiplex bus mode.

Detailed Description

Chip Master Clock Input

The device operates with an external 20MHz OCXO or TCXO as its master clock, connected to the **MCLK** input, pin 99.

The freerun clock may be digitally calibrated from MCLK by writing an offset to the **Freerun_Cal** register, (0x0e/0f), from -102.4 to +102.3 ppm, in 0.1ppm steps, in two's complement form. (See **Register Descriptions** section for details regarding register references in this section.)

Reference Input Monitoring and Qualification

The STC5130 accepts 12 external reference inputs at 8kHz, 64kHz, 1.544MHz, 2.048MHz, 19.44MHz, 38.88MHz, 77.76MHz, 6.48MHz, 8.192MHz, 16.384MHz, 25MHz, or 50MHz. Input frequencies are detected automatically. The autodetected frequency of any reference may be read by selecting the reference in the **Ref_Selector** register (0x15) and then reading the frequency from register **Ref_Frq_Offset** (0x17).

Each input is monitored and qualified for activity and frequency offset. Activity monitoring is accomplished with a leaky bucket accumulation algorithm, as shown in figure 2. The "leaky bucket" accumulator has a fill observation window that may be set from 1 to 16 ms, where any hit of signal abnormality (or multiple hits) during the window increments the bucket count by one. The leak observation window is 1 to 16 times the fill observation window. The leaky bucket accumulator decrements by one for each leak observation window that passes with no signal abnormality. Both windows operate in a consecutive, non-overlapping manner. The bucket accumulator has alarm assert and alarm de-assert thresholds that can each be programmed from 1 to 64.

The fill observation window is written to the **Fill_Obs_Window** register (0x09), and the leak observation window is written to register **Leak_Obs_Window** (0x0a). The bucket size is written to register **Bucket_Size** (0x0b). The alarm assert threshold is written to register **Assert_Threshold** (0x0c), and the de-assert threshold is written to register **De_Assert_Threshold** (0x0d).

Bucket size must be greater than or equal to the alarm assert threshold value, and the alarm assert threshold value must be greater than the alarm de-assert value.

Alarms appear in the **Refs_Activity** register (0x18/19). A "1" indicates activity, and a "0" indicates an alarm, no activity. Note that if a reference is detected as a different frequency, the leaky bucket accumulator is set to the bucket size value and the reference will become inactive immediately.

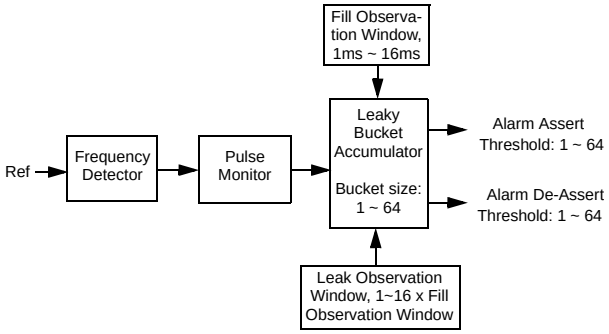


Figure 2: Activity Monitor

Reference inputs are also monitored and qualified for frequency offset.

A reference qualification range may be programmed up to 102.3 ppm by writing to register **Qualification_Range** (0x12/13), and a disqualification range set up to 102.3 ppm, by writing to register **Disqualification_Range** (0x10/11). The qualification range must be set less than the disqualification range. Additionally, a qualification timer may be programmed from 0 to 63 seconds by writing to register **Qualification_Timer** (0x14). The pull-in range is the same as the disqualification range.

The frequency offset (relative to the calibrated freerun clock) of any reference may be read by selecting the reference in the **Ref_Selector** register (0x15) and then reading the offset value from register **Ref_Frq_Offset** (0x16/17).

Figure 3 shows the reference qualification scheme. A reference is qualified if it has no activity alarm and is within the qualification range for more than the qualification time. An activity alarm or frequency offset beyond the disqualification range will disqualify the reference. It may then be re-qualified if the activity alarm is off and the reference is within the qualifica-

tion range for more than the qualification time.

The reference qualification status of each reference may then be read from register **Refs_Qual** (0x1a/ 1b).

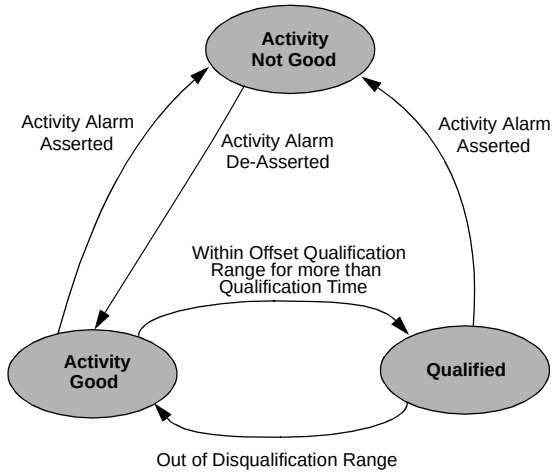


Figure 3: Reference Qualification and Disqualification

DPLL Active Reference Selection

The T0 and T4 clock generators may be individually operated in either manual or automatic input reference selection mode. The mode is selected via the **T0(4)_Control_Mode** registers.

Manual Reference Selection Mode

In manual reference selection mode, the user may select the reference. Manual reference selection mode is selected via the register **T0_Control_Mode** (0x1c) or **T4_Control_Mode** (0x39) (for T0 or T4, respectively) to 0. The reference is selected by writing to the **T0_Manual_Active_Ref** (0x1f) and **T4_Manual_Active_Ref** (0x3c) registers.

Automatic Reference Selection Mode

In automatic reference selection mode, the device will select one pre-qualified reference as the active reference. Automatic reference selection mode is set bthrough the **T0_Control_Mode** (0x1c) or **T4_Control_Mode** (0x39) register (for T0 or T4, respectively).

The reference is picked according to its indicated priority in the reference priority table, registers **T0_Priority_Table** (0x31~0x36) or **T4_Priority_Table** (0x4e ~ 0x53). Each reference has one entry in the table, which may be set to a value from 0 to 15. '0' masks-out the reference, while 1 to 15 set the priority, where '1' has the highest, and '15' has the lowest priority. The highest priority pre-qualified reference may be chosen as the active reference.

The automatically selected reference for each DPLL may be read from registers **T0_Auto_Active_Ref** (0x1e) and **T4_Auto_Active_Ref** (0x3b).

The pre-qualification scheme is described in the **Reference Inputs Monitoring and Qualification** section. When the selected active reference is disqualified, the highest priority qualified remaining reference is chosen. If multiple references share the same priority, they are ordered according to the duration of their qualification. The longer the duration, the higher the priority is set.

When a non-active reference is qualified as the highest priority candidate, it may or may not revert and pre-empt the active reference. This is determined by either enabling or disabling the "revertive" bit of the **T0_Control_Mode** (0x1c) or **T4_Control_Mode** (0x39) register (for T0 or T4, respectively) to "1" for revertive or to "0" for non-revertive operation.

When reversion (pre-emption) is enabled, a reference will be selected immediately as the new active reference, if it becomes the highest priority qualified reference. When reversion is disabled, the current active reference will not be pre-empted by a higher priority reference until it is disqualified.

Digital Phase Locked Loop General Description

The STC5130 includes both a T0 and T4 clock generator. Each clock generator has a DPLL, including a phase detector and a digital filter.

Each clock generator may select any of the 12 input reference clocks in master mode. In slave mode, they will select the **(T0/T4)_XSYNC_IN** cross-couple **SyncLink™** data link and 8kHz data link as the source of phase information.

In master mode, the T0 and T4 clock generators may each operate in the Freerun, Synchronized, or Holdover modes. The transfer into and out of holdover or freerun mode is designed to be smooth and free of hits:

1. Free Run
In freerun mode, the **CLK(0-6)** (**CLK7** for T4) clock outputs are synthesized and may be digitally calibrated from MCLK and have the stability of the external TCXO/OCXO. Reference inputs continue to be monitored for signal presence and frequency offset, but are not used to synchronize the outputs. The transfer into and out of freerun mode is designed to be smooth and free of hits with frequency ramp control.

2. Synchronized
The **CLK(0-6)** (**CLK7** for T4) clock outputs are phase locked to and track the selected input reference. Once satisfactory lock is achieved, the "synchronized" state is entered, and the "SYNC" bit is set in the **T(0/4)_PLL_Status** register.

Each DPLL's loop bandwidth may be set independently. Loop bandwidth is selectable from 90mHz to 107Hz, by writing to the **T0/4_Bandwidth** registers (0x1d/0x3a).

3. Holdover
Upon entering holdover mode, the **CLK(0-6)** (**CLK7** for T4) clock outputs are determined from the holdover history established, or from a user supplied holdover history. The internally accumulated holdover history is a weighted average, with a single-pole low pass filtering algorithm applied, of the frequency offset of the output clocks relative to MCLK (the external TCXO/OCXO). Output clock accuracy in holdover mode is therefore effectively determined by MCLK accuracy.

Holdover mode may be entered manually or automatically. Automatic entry into holdover mode may occur when operating in the automatic mode, the reference is lost, and no other qualified reference exists.

Figure 4 shows the phase locked loop states and transitions for operation with automatic reference selection in Master mode. The transfer into and out of holdover mode is designed to be smooth and free of hits with frequency ramp control.

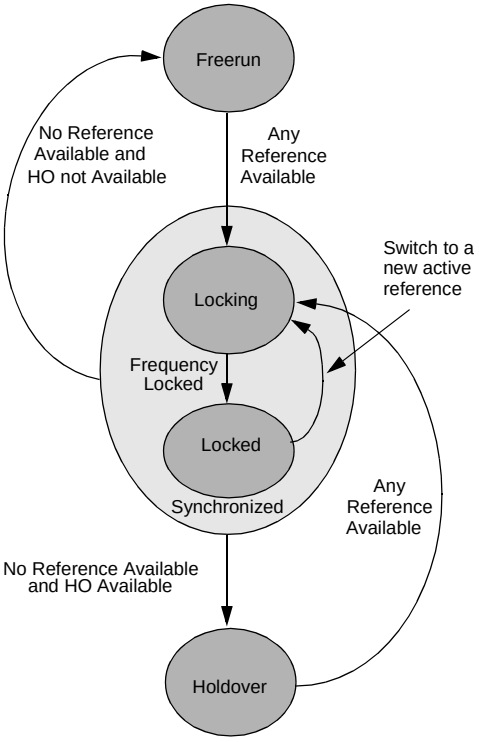


Figure 4: Device phase lock operational mode transition in Automatic Reference Selection/Master Mode

DPLL Operating Mode Details

The T0 and T4 clock generators may operate in the Freerun, Synchronized, or Holdover modes, including some variants thereof:

Freerun Mode

The **CLK(0-6)** (**CLK7** for T4) clock outputs are synthesized and may be digitally calibrated from MCLK and have the stability of the external TCXO/OCXO. The calibration offset may be programmed by the application by writing to the **Freerun_Cal** register, (0x0e/0f). The calibration offset may be programmed from -102.4 to +102.3 ppm, in 0.1ppm steps, in two's complement form.

The Freerun mode may be entered automatically, when in the Automatic Reference Selection mode (as shown in figure 4), or manually, by writing to the **T(0/4)_Manual_Active_Ref** registers.

On all transitions into freerun or back from freerun, an application programmable maximum slew rate of 1, 1.5, or 2 ppm/second (or no slew rate limit) is applied, as written to the **T(0/4)_History_Ramp** registers (0x30/ 0x4d).

Synchronized Mode

The Synchronized mode may be entered automatically, when in the Automatic Reference Selection mode (as shown in figure 4), or manually, by writing to the **T(0/4)_Manual_Active_Ref** registers (0x1f/ 0x3c), selecting a reference as well as the operating mode.

Each DPLL's loop bandwidth may be set independently. Loop bandwidth is selectable from 90mHz to 107Hz by writing to the **T(0/4)_Bandwidth** registers (0x1d/ 0x3a).

In the "Synchronized" mode, "Phase Align Mode" bit of the **T(0/4)_Control_Mode** registers (0x1c, 0x39) determines the output clock to input reference phase alignment mode. In "Arbitrary" mode, the DPLL will be in frequency locking stage initially. When the synchronization achieved ("SYNC" bit will be asserted), the clock output phase relationship relative to the reference input will be reset and locked (phase rebuild). In "Phase Align" mode, the output clocks are phase aligned to the selected reference. (It should be noted that output-to-reference phase alignment is meaningful only in those cases where the output frequency and reference are the same or related by an integer ratio.)

In manual mode selection, there are two special cases of the Synchronized mode:

a) "Zombie" Mode – If the selected active reference signal is lost, the DPLL output is generated according to a short-term history.

b) Out of Pull-in Range Mode - If the selected reference exceeds the pull-in range as programmed by the application, the DPLL output may be programmed to stay at the pull-in range limit, or to follow the reference. This is programmed by writing to "OOP" bit of the **T(0/4)_Control_Mode** registers (0x1c/ 0x39), specifying whether to follow or not follow a reference that has exceeded the pull-in range.

Additionally, when a device is operated as a slave in a master/slave pair (by bringing the **T(0/4)_M/S** pin low), the device locks and phase aligns on the cross-coupled **SyncLink™** data link signal on the **T0_XSYNC_IN** input and the 8kHz signal on the **T4_XSYNC_IN** input.

When the device has locked on a reference, the "SYNC" bit is set in the **T(0/4)_PLL_Status** register (0x37/0x54). If there is a failure to achieve or maintain lock, the "LOL" bit is set in the **T(0/4)_PLL_Status** register.

Holdover Mode

Holdover Mode is analogous to the Freerun mode, except the "frequency offset" is supplied from the holdover history.

The application may select either of two sources of frequency offset in Holdover mode, as determined by writing the "HO_Usage" bit of the **T(0/4)_Control_Mode** registers (0x1c/0x39):

a) Device Accumulated History Holdover Mode – uses the accumulated device holdover history to synthesize the DPLL output.

b) User Supplied History Mode – The DPLL output is synthesized according to an application supplied frequency offset, as provided in the **T(0/4)_User_Accu_History** registers (0x2c/ 0x49). To facilitate the user's accumulation of a holdover history, the user may read the short term history of the active reference from the **T(0/4)_Short_Term_Accu_History** registers (0x28-0x2b/ 0x45-0x48).

Three holdover histories are built:

1) **Short-Term History** – The short-term average frequency of the clock outputs. The weighted single-pole low-pass filter may be programmed for a -3dB point of 2.5, 1.24, 0.62, or 0.31 Hz by writing to the **T(0/**

4)_History_Ramp registers (0x30/0x4d). The short-term history is used in the event of an active reference loss in manual reference selection mode, and may be read from the **T(0/4)_Short_Term_Accu_History** registers (0x28-0x2b/0x45-0x48).

2) **Long-Term History –** The long-term average frequency of the clock outputs, while synchronized to a selected external reference. The weighted single-pole low-pass filter may be programmed for a -3dB point of 9.7, 4.9, 2.4, 1.2, 0.61, or 0.31 mHz, by writing to the **T(0/4)_History_Ramp** registers (0x30/ 0x4d). Internally, an express mode is used after reset by applying a lower time constant for 15 minutes to speed up the history accumulation process. This accumulation process will be reset whenever the selected reference is switched or loss of lock occurs. The accumulation process will then resume after the "SYNC" bit is asserted in the **T(0/4)_DPLL_Status** register (0x37/ 0x54). Additionally, the application may flush/ rebuild this long-term history by writing either "0" or "1" to the **T(0/4)_Accu_Flush** register (0x38/0x55). The long-term history may be read from the **T(0/ 4)_Long_Term_Accu_History** registers (0x24-0x27/0x41-0x44).

3) **Device Holdover History** – This history determines the **CLK(0-6)** (**CLK7** for T4) clock outputs when entering device accumulated history holdover mode. The initial history is zero offset, equal to MCLK, or the uncalibrated freerun frequency. This history will begin to be updated by the long term history after the 15 minute express mode time has completed. Updating will stop if the long term history accumulation process is reset as a result of a reference switch or loss of lock. Thus, the previous holdover history will persist until a new long term history is accumulated following a reference switch or the attendant re-building of the long term history after loss of lock. The "AHR" bit of the **T(0/ 4)_DPLL_Status** registers (0x37/0x54) is set to "1" during updating, but will revert to "0" when updating stops. Additionally, the application may reset this holdover history by writing "1" to the **T(0/4)_Accu_Flush** register (0x38/0x55).

The "HHA" bit of the **T(0/4)_DPLL_Status** registers (0x37/0x54) is asserted "1", indicating the availability of a device holdover history, when the history has been first updated from the long term history or if the user supplied history mode is selected.

On all transitions into holdover or back from holdover, an application programmable maximum slew rate of 1, 1.5, or 2 ppm/second (or no slew rate limit) is applied, as written to the **T(0/4)_History_Ramp** registers (0x30/ 0x4d).

Output Clocks

The clock output section includes 4 clock generators, an APLL, and four dividers, and generates eight synchronized clocks, as shown in figure 5.

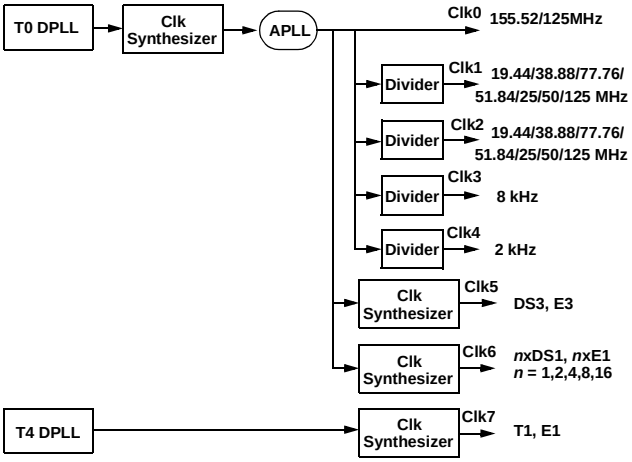


Figure 5: Output Clocks

The first synthesizer drives an analog PLL and generates five output clocks. It is driven from the T0 DPLL:

- **CLK0**: 155.52/125 MHz (LVDS), selected or disabled by writing the **CLK0_Sel** register (0x56), bits 0 - 1.
- **CLK1**: Programmable at 19.44MHz, 38.88MHz, 51.84MHz, 77.76 MHz, 25MHz, 50MHz, 125MHz, and disabled, by writing to the **CLK1_Sel** register (0x57), bits 0 - 2.
- **CLK2**: Programmable at 19.44MHz, 38.88MHz, 51.84, 77.76 MHz, 25MHz, 50MHz, 125MHz, and disabled, by writing to the **CLK2_Sel** register (0x58), bits 0 - 2.
- **CLK3**: 8kHz, 50% duty cycle or programma-

ble pulse width, and may be disabled by writing to the **CLK3_Sel** register (0x59), bits 0 - 5.

- **CLK4**: 2kHz, 50% duty cycle or programmable pulse width, and may be disabled by writing to the **CLK4_Sel** register (0x5a), bits 0 - 5.

Two synthesizers generate additional clocks from the T0 clock generator:

- **CLK5**: Either DS3 or E3 rate, or "disabled", programmed by writing to the **CLK5_Sel** register (0x5b), bits 0 - 1.
- **CLK6**: Programmable at nxDS1 or nxE1 rate, where n=1,2,4,8,16, or may be disabled, by writing to the **CLK6_Sel** register (0x5c), bits 0 - 3.

One synthesizer is driven by the T4 clock generator:

- **CLK7**: Either DS1 or E1 rate, or "disabled", programmed by writing to the **CLK7_Sel** register (0x5d), bits 0 - 1.

When a clock output is disabled, the pin is tri-stated.

In addition, the **T0_XSYNC_OUT** output provides phase information and state data for master/slave operation of the T0 clock generators. The **T4_XSYNC_OUT** output provides an 8kHz signal for master/slave operation of the T4 clock generator.

Note that **CLK0,1, 2, 5** and **6** are phase aligned with **CLK3** (8kHz) as shown in Figure 7. **CLk3** is phase aligned with **CLK4** (2kHz).

Master/Slave Configuration

Pairs of STC5130 devices may be operated in a master/slave configuration for added reliability, as shown in Figure 6.

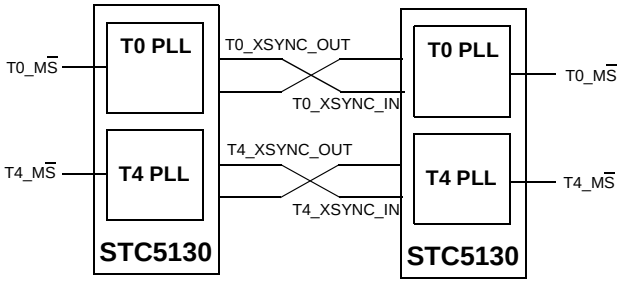


Figure 6: Master/Slave Configuration

Devices are configured for master/slave operation by cross-connecting their respective **T(0/4)_XSYNC_OUT** and/or **T(0/4)_XSYNC_IN** pins. The **T(0/4)_MS** pins determine the master or slave mode for each clock generator. 1=Master, 0=Slave. Thus, master/slave state is always manually controlled by the application. The slave T0 synchronizes and phase-aligns in the 2kHz domain according to data received over the **T0_XSYNC_OUT** / **T0_XSYNC_IN** data link from the unit in master mode. The slave T4 synchronizes and phase-aligns to the 8kHz received on the **T4_XSYNC_OUT** / **T4_XSYNC_IN** connection from the unit in master mode.

The T0 and T4 may be operated completely independent of each other – either or both may be cross-connected as master/slave pairs across two STC5130 devices, and master/slave states may be set the same or opposite within a given device.

While in the slave configuration, the operational mode is “synchronized”. The **T(0/4)_XSYNC_OUT** data link/8kHz signals provide the phase information of 2kHz (T0) and 8kHz (T4) for phase alignment between the master and the slave. In addition to phase information, **T0_XSYNC_OUT** also provides the reference selection state to ensure that later the new master may lock on the same reference if reference selection is in “automatic” mode.

The **T0_T4_MS_Sts** register reflect the states of the **T(0/4)_MS** pins.

Master/Slave Operation

Perfect phase alignment of the **Clk(x)** output clocks (between the clock generators in two devices) would require no delay on the cross-couple data link connection. To accommodate path length delays, the STC5130 provides a programmable phase skew feature. See figures 7 and 8. The slave’s **Clk(x)** outputs may be phase shifted from 0 to +409.5ns, in 100ps increments according to the contents of the **T(0/4)_Slave_Phase_Adj** (0x05/06, 0x07/08) registers to compensate for the path length of the **T(0/4)_XSYNC_OUT** to **T(0/4)_XSYNC_IN** connections. This offset may therefore be programmed to exactly compensate for the actual path length delay associated with the particular application's cross-couple traces. Thus, master/slave switches with the STC5130 devices may be accomplished with near-zero phase hits.

The first time a clock generator becomes a slave, such as immediately after power-up, its output clock phase starts out arbitrary, and will quickly phase-align to the master unit. The phase skew will be eliminated (or converged to the programmed phase offset) step by step. The whole pull-in-and-lock process will complete in about 16 seconds. There is no frequency slew protection in slave mode. In slave mode, the unit's mission is to lock to and follow the master.

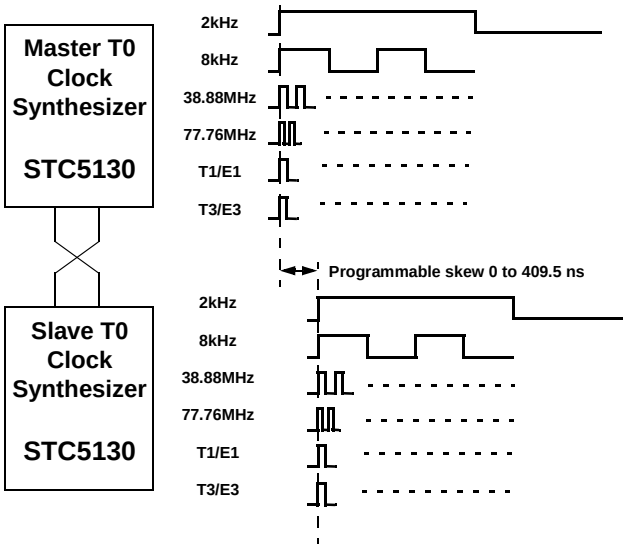


Figure 7: T0 **CLK1-6** Phase Alignment and Master/Slave skew Control

Activity of the signals on the **T(0/4)_XSYNC_IN** pins is available in the **Refs_Activity** register (0x18/19). (The leaky bucket algorithms are not applied to these signals.)

Note the phase alignment of all clock outputs from the T0 clock generator with the 2kHz output.

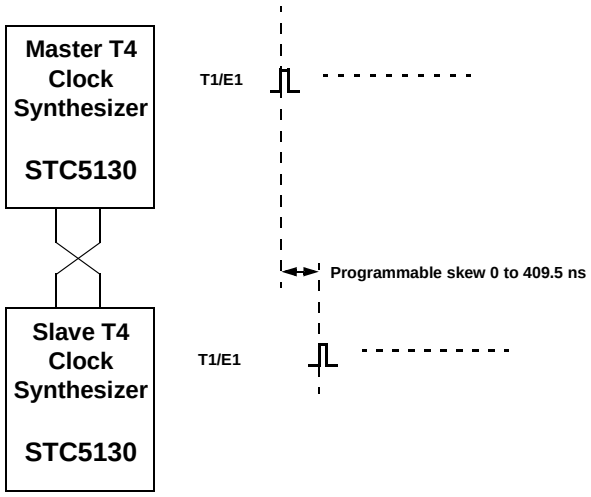


Figure 8: T4 **CLK7** Master/Slave Skew Control

Once a pair of clock generators has been operating in aligned master/slave mode, and a master/slave switch occurs, the clock generator that becomes master will maintain its output clock phase and frequency while a phase rebuild (to the current output clock phase) is performed on its selected reference input. Therefore, as master mode operation commences, there will be no phase or frequency hits on the clock output. Assuming the phase offset is programmed for the actual propagation delay of this cross-couple path, there will again be no phase hits on the output clock of the clock generator that has transitioned from master to slave.

Processor Interface Descriptions

The STC5130 supports four common microprocessor control interfaces: SPI, Motorola, Intel, and multiplex parallel. The control interface mode is selected with the **Bus_Mode(0/1)** pins:

Bus_Mode1	Bus_Mode0	Bus Mode
0	0	SPI
0	1	Multiplex parallel
1	0	Intel
1	1	Motorola

The following sections describe each bus mode's interface timing:

SPI Bus Mode

The SPI interface bus mode uses the $\overline{\text{BUS\_CS}}$, BUS_ALE, BUS_RDB, and BUS_RDY pins, corresponding to CS, SCLK, SDI, and SDO respectively, with timing as shown in figures 9 and 10:

Serial Bus Timing

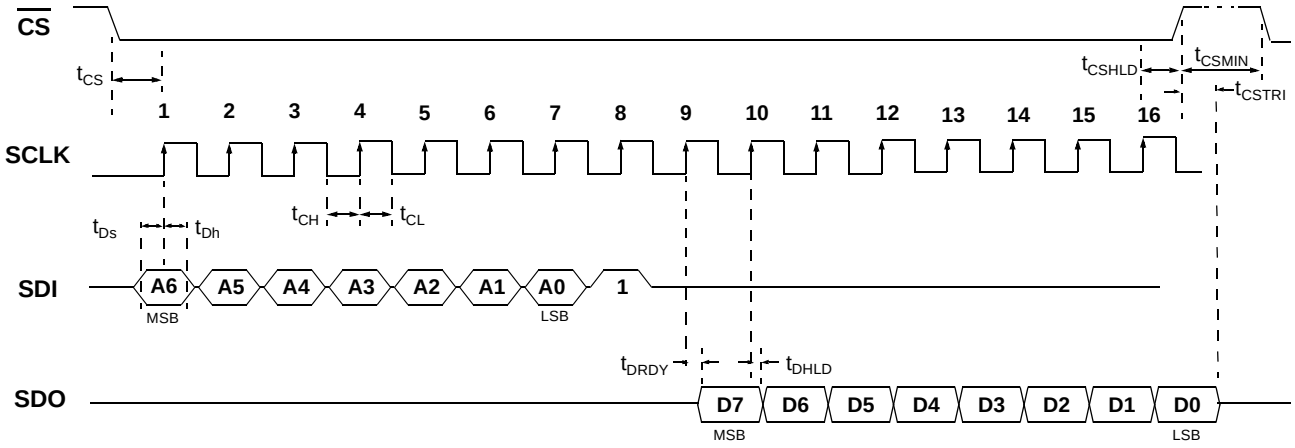


Figure 9: Serial Bus Timing, Read access

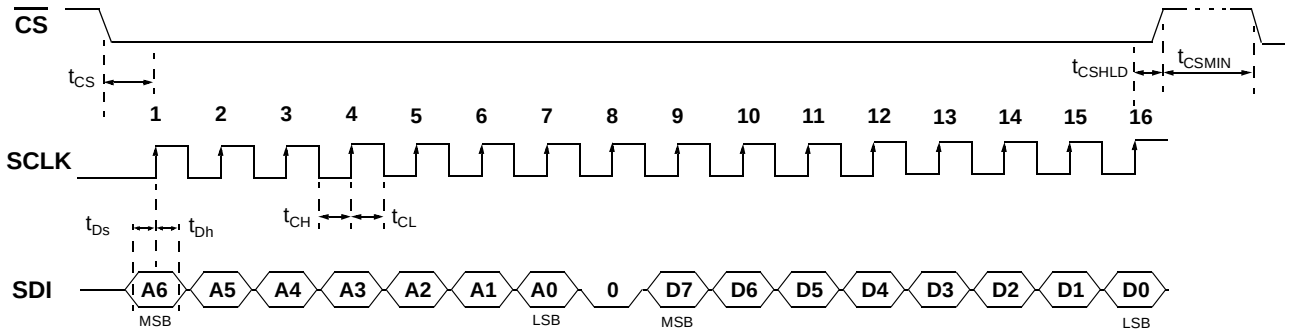


Figure 10: Serial Bus Timing, Write access

Table 5: Serial Bus Timing

Symbol	Description	Min	Max	Unit
t_{CS}	$\overline{CS}$ low to SCLK high	10		ns
t_{CH}	SCLK high time	25		ns
t_{CL}	SCLK low time	25		ns
t_{Ds}	Data setup time	10		ns
t_{Dh}	Data hold time	10		ns
t_{DRDY}	Data ready		7	ns
t_{DHLD}	Data hold	3		ns
t_{CSHLD}	Chip select hold	30		ns
t_{CSTRI}	Chip select to data tri-state		5	ns
t_{CSMIN}	Minimum delay between successive accesses	50		ns

Motorola Bus

In Motorola mode, the device will interface to 680xx type processors. The BUS_CS, BUS_RDB, BUS_A(6-0), BUS_AD(7-0), and BUS_RDY pins are used, corresponding to CS, R/W, A, AD, and RDY, respectively. Timing is as follows:

Motorola Bus Timing

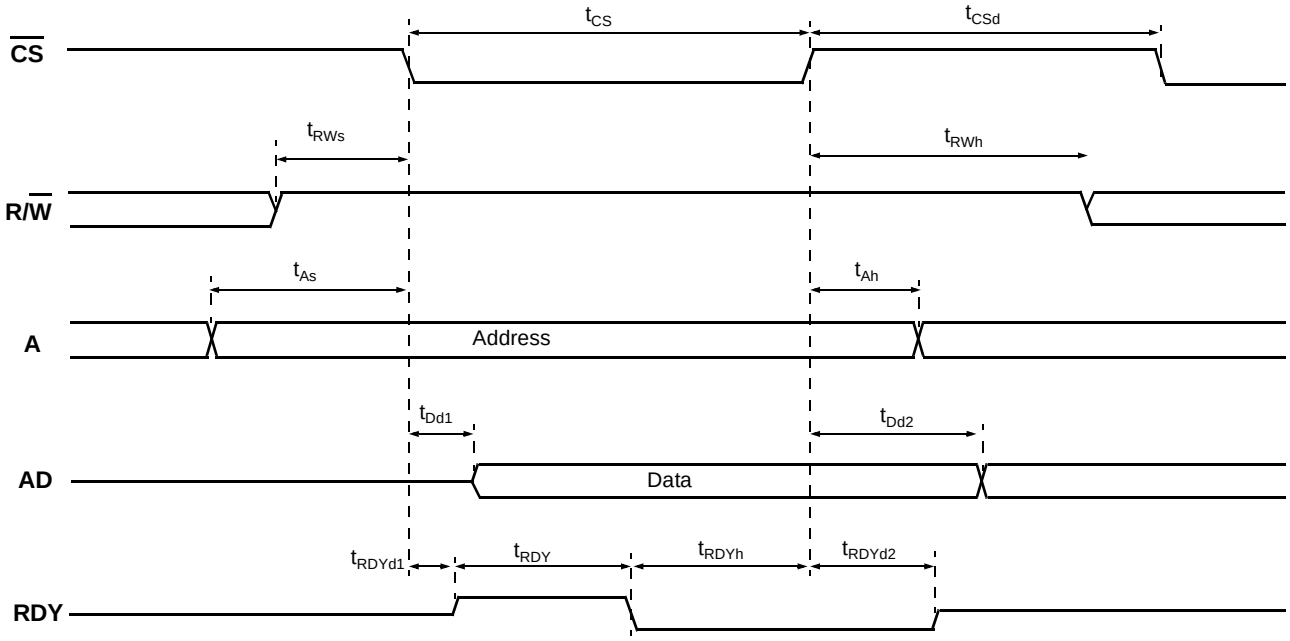


Figure 11: Motorola Bus Read Timing

Table 6: Motorola Bus Read Timing

Symbol	Description	Min	Max	Unit
t_{CS}	$\overline{CS}$ low time	50		ns
t_{CSd}	$\overline{CS}$ minimum high time between reads/writes	50		ns
t_{RWs}	Read/write setup time	0		ns
t_{RWh}	Read/write hold time	0		ns
t_{As}	Address setup	10		ns
t_{Ah}	Address hold	0		ns
t_{Dd1}	Data valid delay from $\overline{CS}$ low		50	ns
t_{Dd2}	Data high-z delay from $\overline{CS}$ low		10	ns
t_{RDY1}	$\overline{CS}$ low to RDY high delay		13	ns
t_{RDY}	RDY high time	37	50	ns
t_{RDYh}	$\overline{CS}$ hold after RDY low	0		ns
t_{RDY2}	RDY high-z delay after $\overline{CS}$ high		9	ns

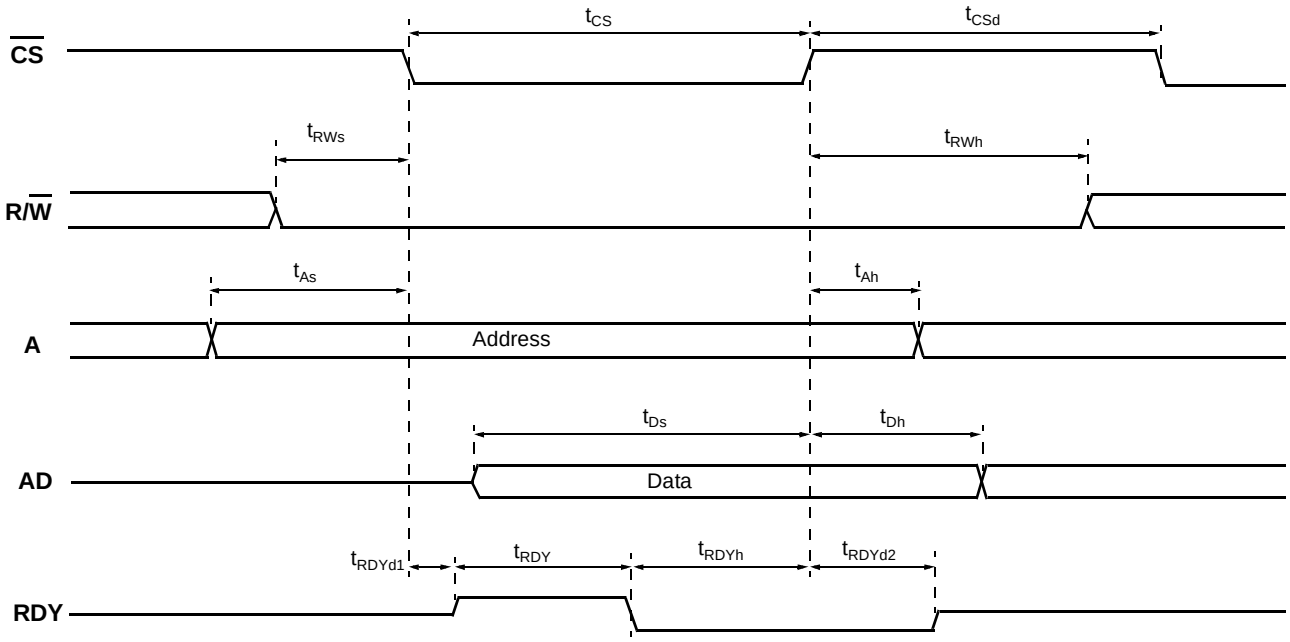


Figure 12: Motorola Bus Write timing

Table 7: Motorola Bus Read Timing

Symbol	Description	Min	Max	Unit
t_{CS}	$\overline{CS}$ low time	50		ns
t_{CSd}	$\overline{CS}$ minimum high time between writes/reads	50		ns
t_{RWs}	Read/write setup time	0		ns
t_{RWh}	Read/write hold time	0		ns
t_{As}	Address setup	10		ns
t_{Ah}	Address hold	0		ns
t_{Ds}	Data setup time before $\overline{CS}$ high	10		ns
t_{Dh}	Data hold time after $\overline{CS}$ high	10		ns
t_{RDYd1}	$\overline{CS}$ low to RDY high delay		13	ns
t_{RDY}	RDY high time	37		ns
t_{RDYh}	$\overline{CS}$ hold after RDY low	0		ns
t_{RDYd2}	RDY high-z delay after $\overline{CS}$ high		7	ns

Intel Bus

In Intel mode, the device will interface to 80x86 type processors. The BUS_CS, BUS_WRB, BUS_RDB, BUS_A(6-0), BUS_AD(7-0), and BUS_RDY pins are used, corresponding to CS, WRB, RDB, A, AD, and RDY, respectively. Timing is as follows:

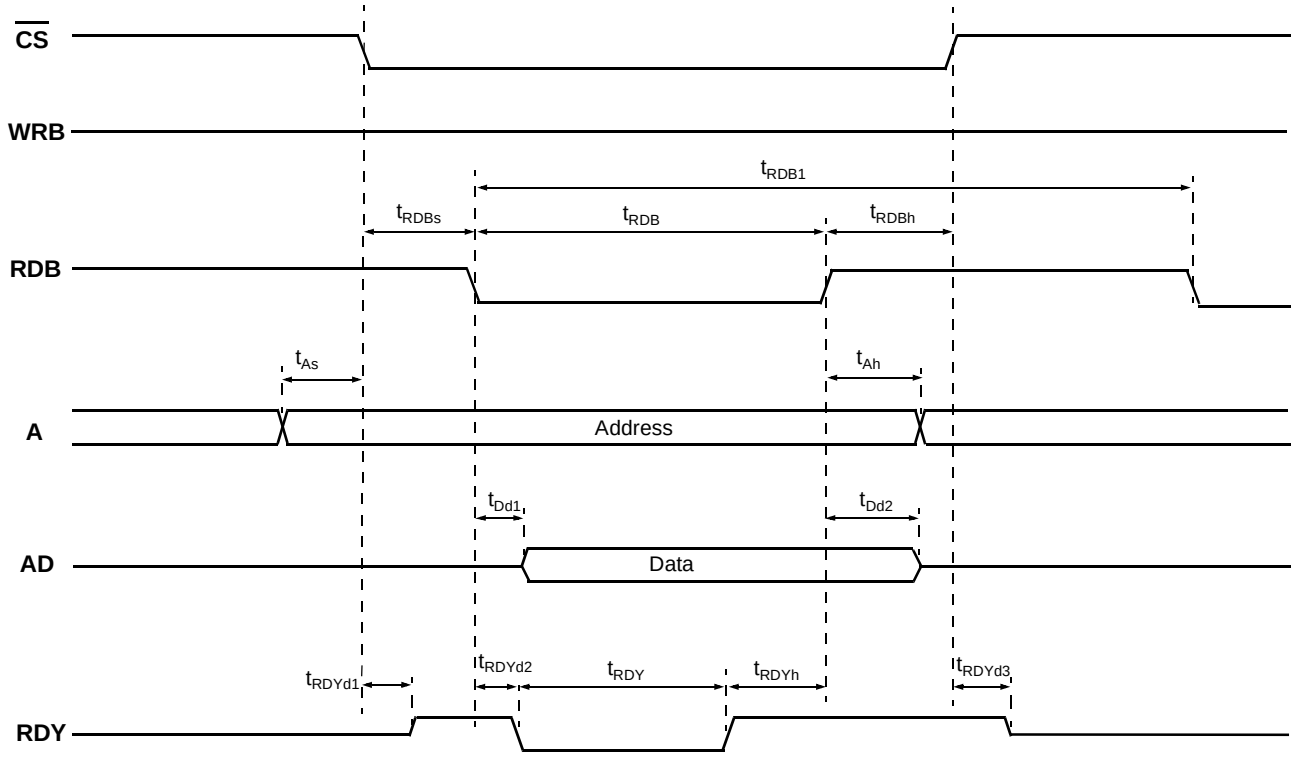


Figure 13: Intel Bus Read Timing

Table 8: Intel Bus Read Timing

Symbol	Description	Min	Max	Unit
t_{RDBs}	Read setup time	0		ns
t_{RDB}	Read low time	40		ns
t_{RDBh}	Read hold time	0		ns
t_{RDB1}	Time between consecutive reads	50		ns
t_{As}	Address setup	10		ns
t_{Ah}	Address hold	0		ns
t_{Dd1}	Data valid delay from RDB high		50	ns
t_{Dd2}	Data high-z delay from RDB high		10	ns
t_{RDYd1}	$\overline{CS}$ low to RDY high delay		13	ns
t_{RDYd2}	RDB low to RDY low		40	ns
t_{RDY}	RDY low time	50		ns
t_{RDYh}	RDB hold after RDY high	0		ns
t_{RDY3}	RDY high-z delay after $\overline{CS}$ high		11	ns

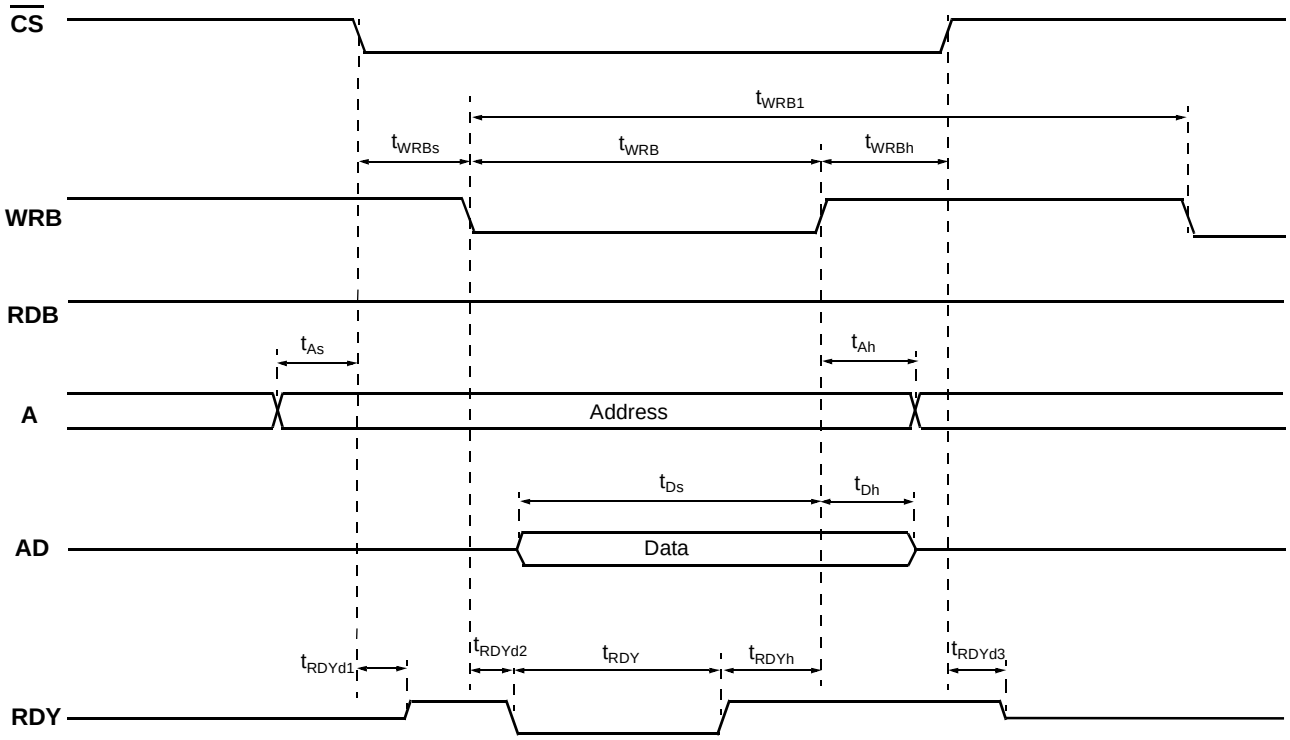


Figure 14: Intel Write Read Timing

Table 9: Intel Bus Write Timing

Symbol	Description	Min	Max	Unit
t_{WRBs}	Write setup time	0		ns
t_{WRB}	Write low time	40		ns
t_{WRBh}	Write hold time	0		ns
t_{WRB1}	Time between consecutive writes	50		ns
t_{As}	Address setup	10		ns
t_{Ah}	Address hold	0		ns
t_{Ds}	Data setup time before $\overline{CS}$ high	10		ns
t_{Dh}	Data hold time after $\overline{CS}$ high	10		ns
t_{RDYd1}	$\overline{CS}$ low to RDY high delay		13	ns
t_{RDYd2}	RDB low to RDY low		40	ns
t_{RDY}	RDY low time	50		ns
t_{RDYh}	RDB hold after RDY high	0		ns
t_{RDY3}	RDY high-z delay after $\overline{CS}$ high		10	ns

Multiplex Bus Mode

In multiplex bus mode, the device can interface with microprocessors which share the address and data on the same bus signals. The BUS_ALE, BUS_CS, BUS_WRB, BUS_RDB, BUS_AD(7-0), and BUS_RDY pins are used, corresponding to ALE, CS, WRB, RDB, AD, and RDY, respectively.

Multiplex Bus Timing

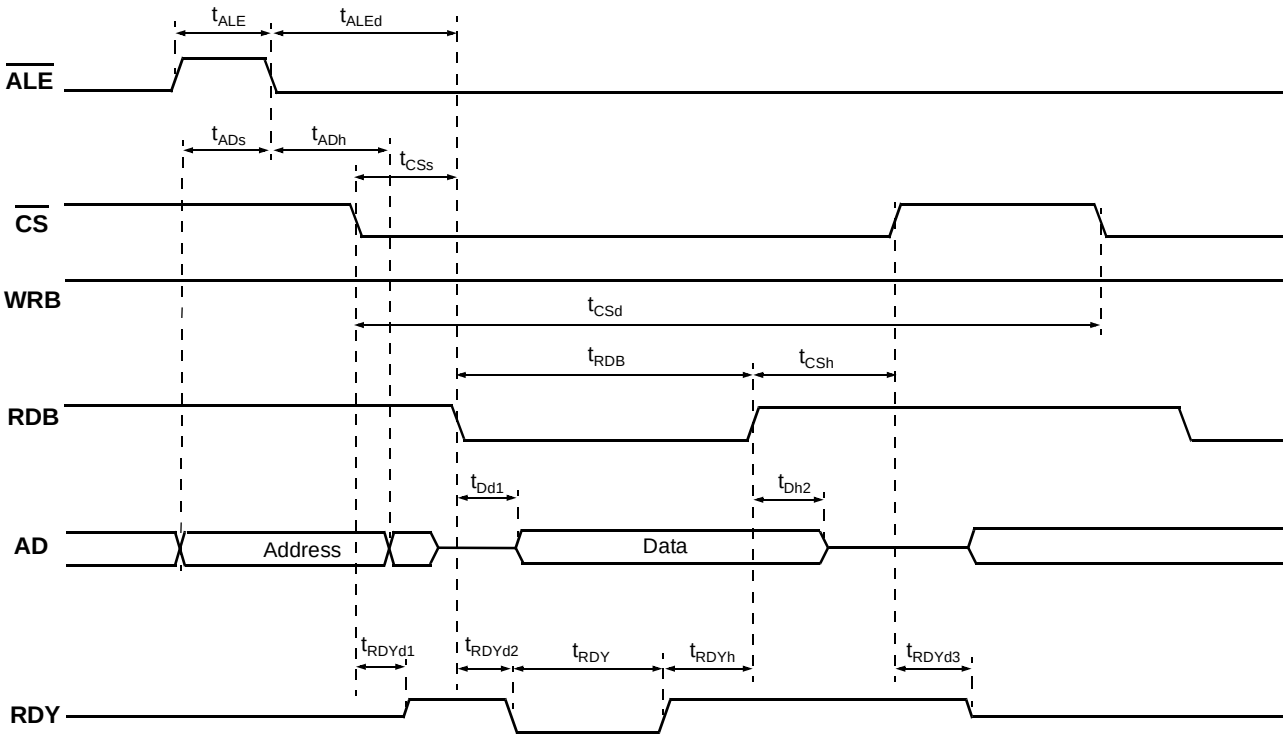


Figure 15: Multiplex Bus Read Timing

Table 10: Multiplex Bus Read Timing

Symbol	Description	Min	Max	Unit
t_{ALE}	ALE high time	10		ns
t_{ALEd}	ALE falling edge to RDB low	0		ns
t_{ADs}	Address setup time	10		ns
t_{ADh}	Address hold time	10		ns
t_{CSs}	Read setup time	0		ns
t_{RDB}	Read time	40		ns
t_{CSh}	$\overline{CS}$ hold time	0		ns
t_{CSd}	$\overline{CS}$ delay for multiple read/writes	50		ns
t_{Dd1}	Data valid delay from RDB low		50	ns
t_{Dh2}	Data high-z from RDB high		10	ns
t_{RDYd1}	$\overline{CS}$ low to RDY active		13	ns
t_{RDYd2}	RDB low to RDY low		40	ns
t_{RDY}	RDY low time	50		ns
t_{RDYh}	Read hold after RDY high	0		ns
t_{RDYd3}	RDY high-z delay after $\overline{CS}$ high		10	ns

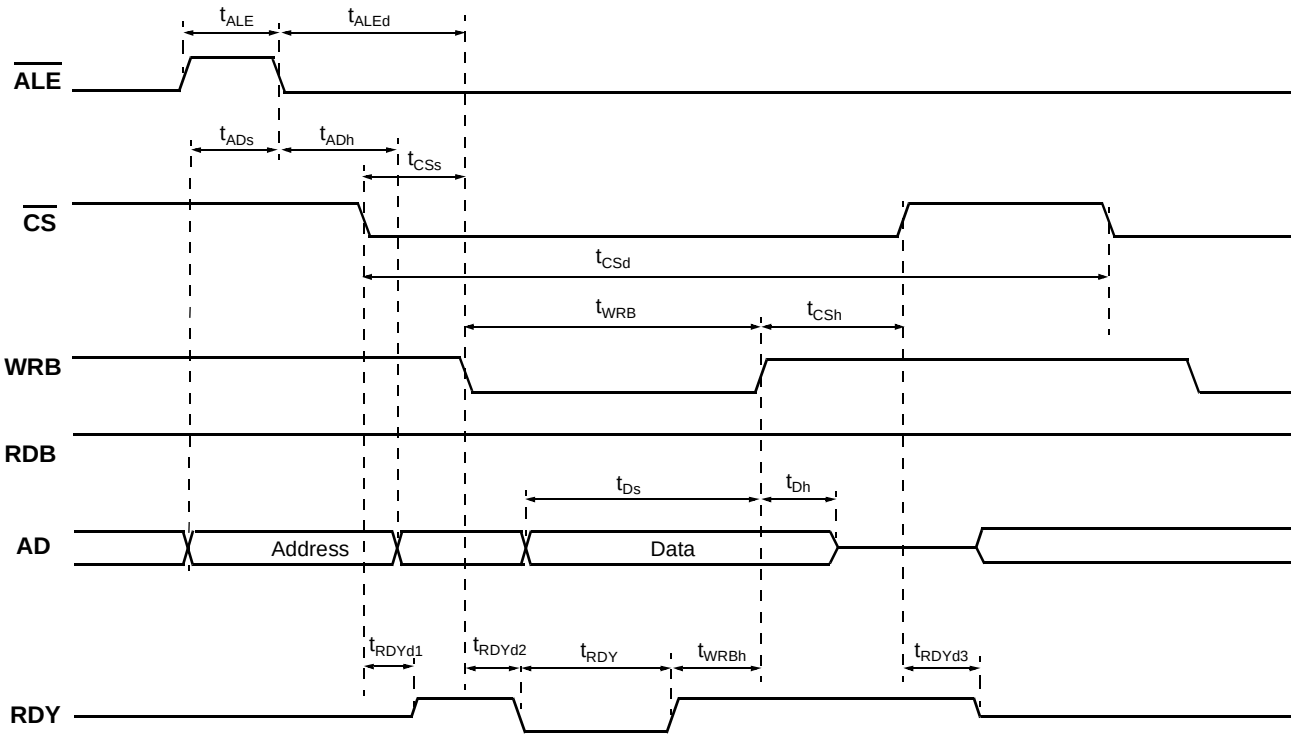


Figure 16: Multiplex Bus Write Timing

Table 11: Multiplex Bus Write Timing

Symbol	Description	Min	Max	Unit
t_{ALE}	ALE high time	10		ns
t_{ALEd}	ALE falling edge to RDB low	0		ns
t_{ADs}	Address setup time	10		ns
t_{ADh}	Address hold time	10		ns
t_{CSs}	Write $\overline{CS}$ setup time	0		ns
t_{WRB}	Write time	40		ns
t_{CSh}	$\overline{CS}$ hold time	10		ns
t_{CSd}	$\overline{CS}$ delay for multiple write/reads	50		ns
t_{Ds}	Data setup time	10		ns
t_{Dh}	Data hold time	10		ns
t_{RDYd1}	$\overline{CS}$ low to RDY active		13	ns
t_{RDYd2}	WRB low to RDY low		40	ns
t_{RDY}	RDY low time	50		ns
t_{WRBh}	WRB hold after RDY high	0		ns
t_{RDYd3}	RDY high-z delay after $\overline{CS}$ high		9	ns

Register Descriptions and Operation

General Register Operation

The STC5130 device has 1, 2, and 4 byte registers. One byte registers are read and written directly. Two and four byte registers must be read and written in a specific manner and order, as follows:

Multibyte register reads

A multibyte register read must commence with a read of the least significant byte first. This triggers a transfer of the remaining byte(s) to a holding register, ensuring that the remaining data will not change with the continuing operation of the device. The remaining byte(s) must be read consecutively with no intervening read/writes from/to other registers.

Multibyte register writes

A multibyte register write must commence with a write to the least significant byte first. Subsequent writes to the remaining byte(s) must be performed in ascending byte order, consecutively, with no intervening read/writes from/to other registers, but with no timing restrictions. Multibyte register writes are temporarily stored in a holding register, and are transferred to the target register when the most significant byte is written.

Clearing bits in the Interrupt Status Register

Interrupt event register (**Intr_Event**, 0x5e~0x5f) bits are cleared by writing a “1” to the bit position to be cleared. Interrupt bit positions to be left as is are written with a “0”.

Chip_ID, 0x00 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x00	0x30							
0x01	0x51							

Chip_Rev, 0x02 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x02	Revision Number							

Chip_Sub_Rev, 0x03 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x03	Sub-Revision Number							

T0_T4_MS_Sts, 0x04 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x04	Not used						T4 M/S	T0 M/S

Reflects the states of the **T0/T4_MASTER_SLAVE** select pins. 1 = Master, 0 = slave

T0_Slave_Phase_Adj, 0x05 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x05	Adjust T0 slave phase from 0 ~ 409.5 ns in 0.1 ns steps, lower 8 bits							
0x06	Not used				Adjust T0 slave phase from 0 ~ 409.5 ns in 0.1 ns steps, upper 4 bits			

The T0 slave phase may be adjusted 0 to 409.5 ns relative to the cross couple input with 0.1 ns resolution. This is a 12 bit register, split across address 0x05 and 0x06.
Default value: 0

T4_Slave_Phase_Adj, 0x07 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x07	Adjust T4 slave phase from 0 ~ 409.5 ns in 0.1 ns steps, lower 8 bits							
0x08	Not used				Adjust T4 slave phase from 0 ~ 409.5 ns in 0.1 ns steps, upper 4 bits			

The T4 slave phase may be adjusted 0 to 409.5 ns relative to the cross couple input with 0.1 ns resolution. This is a 12 bit register, split across address 0x07 and 0x08.
Default value: 0

Fill_Obs_Window, 0x09 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x09	Not used				Leaky bucket fill observation window, *m* = 0 ~ 15			

Sets the fill observation window size for the reference activity monitor to (*m*+1) ms. The window size can be set from 1ms to 16ms.
Default value: *m* = 0, (1ms)

Leak_Obs_Window, 0x0a (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0a	Not used				Leaky bucket fill observation window, *n* = 0 ~ 15			

Sets the leak observation window size for the reference activity monitor to (*n* + 1) times the fill observation window size.
Default value: *n* = 3, (4 times)

Bucket_Size, 0x0b (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0b	Not used		Leaky bucket size, 1 ~ 63					

Sets the leaky bucket size for the reference activity monitor. Bucket size must be greater than or equal to the alarm assert value. Invalid values will not be written to the register.
Default value: 20

Assert_Threshold, 0x0c (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0c	Not used		Leaky bucket alarm assert threshold, 1 ~ 63					

Sets the leaky bucket alarm assert threshold for the reference activity monitor. The alarm assert threshold value must be greater than the de-assert threshold value and less than or equal to the bucket size value. Invalid values will not be written to the register.
Default value: 15

De_Assert_Threshold, 0x0d (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0d	Not used		Leaky bucket alarm de-assert threshold, 0 ~ 62					

Sets the leaky bucket alarm de-assert threshold for the reference activity monitor. The de-assert threshold value must be less than the assert threshold value. Invalid values will not be written to the register.
Default value: 10

Freerun_Cal, 0x0e (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0e	Lower 8 bits							
0x0f	Not used					Upper 3 bits		

Freerun calibration, from -102.4 to +102.3 ppm, in 0.1ppm steps, two's complement.
Default value: 0

Disqualification_Range, 0x10 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x10	Lower 8 bits							
0x11	Not used						Upper 2 bits	

Reference disqualification range, from 0 to +102.3 ppm, in 0.1 ppm steps. This also sets the pull-in range. (See the **Reference Input Monitoring and Qualification** section)
Default value: 110 (range = 11.0 ppm).

Qualification_Range, 0x12 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x12	Lower 8 bits							
0x13	Not used						Upper 2 bits	

Reference qualification range, from 0 to +102.3 ppm, in 0.1 ppm steps.
Default value: 100 (range = 10.0 ppm).

Qualification_Timer, 0x14 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x14	Not used		0 ~ 63 s					

Reference qualification timer, from 0 to 63 s.
Default value: 10

Ref_Selector, 0x15 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x15	Not used				1 ~ 12 (0x1 ~ 0xc)			

Determines which reference data is displayed in register 0x16 and 0x17. Valid values from 1 to 12. Invalid values will not be written to the register.
Default value: 1

Ref_Frq_Offset, 0x16 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x16	Lower 8 bits of frequency offset							
0x17	Reference frequency				Upper 4 bits of frequency offset			

Displays the frequency offset and reference frequency for the reference selected by the **Ref_Selector** (0x15) register. Frequency offset is from -204.7 to +204.7 ppm relative to calibrated freerun, in 0.1 ppm steps, two's complement. A value of -2048 indicates the reference is out of range.

The reference frequency is determined as follows ("Unknown" indicates a signal is present, but frequency is undetermined):

0x17, bits 7 ~ 4	Frequency
0	No signal
1	8 kHz
2	64 kHz
3	1.544 MHz
4	2.048 MHz
5	19.44 MHz
6	38.88 MHz
7	77.76 MHz
8	6.48MHz

0x17, bits 7 ~ 4	Frequency
9	8.192MHz
10	16.384MHz
11	25 MHz
12	50 MHz
13	Reserved
14	Unknown
15	Reserved

Refs_Activity, 0x18 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x18	Ref 8	Ref 7	Ref 6	Ref 5	Ref 4	Ref 3	Ref 2	Ref 1
0x19	Not used		T4_XSYNC_IN	T0_XSYNC_IN	Ref 12	Ref 11	Ref 10	Ref 9

Reference activity indicator, 0 = no activity, 1 = activity.

Refs_Qual, 0x1a (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1a	Ref 8	Ref 7	Ref 6	Ref 5	Ref 4	Ref 3	Ref 2	Ref 1
0x1b	Not used				Ref 12	Ref 11	Ref 10	Ref 9

Reference qualification indicator, 0 = not qualified, 1 = qualified.

T0_Control_Mode, 0x1c (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1c	Not used		OOP: Out of Pull-in range: 0=Follow 1=Don't follow	Manual/ Auto 0=Manual 1=Auto	Revertive 0=Non-revertive 1=Rever-tive	HO_Usage 0=DHH 1=User	Not used	Phase Align Mode 0=Arbitrary 1=Align

Mode control bits for T0.

Bit 0: 0 = Arbitrary (use initial phase), 1 = Phase align

Bit 2, HO_Usage: 0 = Device Holdover History (DHH) is used; 1 = User supplied history is used.

Bit 5, OOP: In manual mode, when the selected active reference is out of the pull-in range, as specified in register **Disqualification_Range**, 0x10, OOP will determine if the reference is to be followed, 0 = Follow, 1 = Don't follow.

Default value: 0

T0_Bandwidth, 0x1d (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1d	Not used			Bandwidth select				

Sets the T0 loop bandwidth:

0x1d, bits 4 ~ 0	Bandwidth, Hz
0	107
1	50
2	24
3	12
4	5.9
5	2.9
6	1.5
7	.73
8	0.37
9	0.18
10	0.09
31 ~ 11	Reserved

Default value: 6

T0_Auto_Active_Ref, 0x1e (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1e	Not used				Selection			

Indicates the automatically selected active reference for T0, when this T0 is a “master”. When this T0 is a “slave”, the master’s active reference is indicated. (Data valid in automatic mode only)

Bit 3 ~ Bit 0	Selection
0	Freerun
1 ~ 12	Sync with Ref 1 ~ Ref 12
13	Holdover
14, 15	Reserved

T0_Manual_Active_Ref, 0x1f (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1f	Not used				Selection			

Selects the active reference for T0 in manual reference select mode.

Bit 3 ~ Bit 0	Selection
0	Freerun
1 ~ 12	Sync with Ref 1 ~ Ref 12
13	Holdover
14, 15	Reserved

Default value: 0

T0_Device_Holdover_History, 0x20 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x20	Bits 0 - 7 of 32 bit Device Holdover History							
0x21	Bits 8 - 15 of 32 bit Device Holdover History							
0x22	Bits 16 - 23 of 32 bit Device Holdover History							
0x23	Bits 24 - 31 of 32 bit Device Holdover History							

Device holdover history for T0 relative to MCLK. 2's complement. Resolution is 0.745×10^{-3}ppb.
Default value: 0

T0_Long_Term_Accu_History, 0x24 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x24	Bits 0 - 7 of 32 bit Long Term History							
0x25	Bits 8 - 15 of 32 bit Long Term History							
0x26	Bits 16 - 23 of 32 bit Long Term History							
0x27	Bits 24 - 31 of 32 bit Long Term History							

Long term accumulated history for T0 relative to MCLK. 2's complement. Resolution is 0.745×10^{-3} ppb.

T0_Short_Term_Accu_History, 0x28 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x28	Bits 0 - 7 of 32 bit Short Term History							
0x29	Bits 8 - 15 of 32 bit Short Term History							
0x2a	Bits 16 - 23 of 32 bit Short Term History							
0x2b	Bits 24 - 31 of 32 bit Short Term History							

Short term accumulated history for T0 relative to MCLK. 2's complement. Resolution is 0.745×10^{-3} ppb.

T0_User_Accu_History, 0x2c (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x2c	Bits 0 - 7 of 32 bit User Holdover History							
0x2d	Bits 8 - 15 of 32 bit User Holdover History							
0x2e	Bits 16 - 23 of 32 bit User Holdover History							
0x2f	Bits 24 - 31 of 32 bit User Holdover History							

User accumulated history for T0 relative to MCLK. 2's complement. Resolution is 0.745×10^{-3} ppb.
Default value: 0

T0_History_Ramp, 0x30 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x30	Not used	Long Term History Bandwidth			Short Term History Band-width		Ramp control	

Holdover bandwidth and ramp controls for T0:

0x30, bits 6 ~ 4	Long Term History -3dB Bandwidth
000	9.7 mHz
001	4.9 mHz
010	2.4 mHz
011	1.2 mHz
100	0.61 mHz
101	0.30 mHz

0x30, bits 3 ~ 2	Short Term History -3dB Bandwidth
00	2.5 Hz
01	1.24 Hz
10	0.62 Hz
11	0.31 Hz

0x30, bits 1 ~ 0	Ramp control
00	No Control
01	1 ppm/s
10	1.5 ppm/s
11	2 ppm/s

Default value: 0x27 (2.4mHz; 1.24Hz; 2ppm/s)

T0_Priority_Table, 0x31 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x31	Ref 2 Priority				Ref 1 Priority			
0x32	Ref 4 Priority				Ref 3 Priority			
0x33	Ref 6 Priority				Ref 5 Priority			
0x34	Ref 8 Priority				Ref 7 Priority			
0x35	Ref 10 Priority				Ref 9 Priority			
0x36	Ref 12 Priority				Ref 11 Priority			

Reference priority for automatic reference selection mode. Lower values have higher priority:

0x31 - 0x36, 4 bits	Reference Priority
0000	Disable reference
0001 ~ 1111	1 ~ 15

Default value: 0

T0_PLL_Status, 0x37 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x37	HHA 1=Available 0=Not available	AHR 1=Ready 0=Not ready	Reserved	SAP 1=Stop at pull-in range 0=Follow-ing	OOP 1=Out of pull-in range 0=In range	LOL 0=No LOL 1=LOL	LOS 0=No LOS 1=LOS	SYNC: 0=No Sync 1=Sync

SYNC: Indicates synchronization has been achieved
LOS: Loss of signal of the active reference
LOL: Loss of lock (Failure to achieve or maintain lock)
OOP: Out of pull-in range
AHR: Active Holdover History Ready
HHA: Holdover History Available
SAP: Indicates the output clocks stop following the selected reference, caused by out of pull-in range

HHA	AHR	Holdover Status
1	1	Holdover History available: Device Holdover History tracking on the current active reference
1	0	Holdover History available: Device Holdover History based on last available history
0	0	Holdover History not available
0	1	Not applicable

T0_Accu_Flush, 0x38 (W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x38	Not used							HO flush

Writing to this register will perform a flush of the accumulated history. The value of bit zero determines which histories are flushed. Bit 0 = 0, Flush and reset T0 long term history only; bit 0 = 1, flush/reset both T0 long term history and the T0 device holdover history.

T4_Control_Mode, 0x39 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x39	Not used		OOP: Out of Pull-in range: 0=Follow 1=Don't fol-low	Manual/ Auto 0=Manual 1=Auto	Revertive 0=Non-revertive 1=Rever-tive	HO_Usage 0=DHH 1=User	Not used	Phase Align Mode 0=Arbitrary 1=Align

Mode control bits for T4.

Bit 0: 0 = Arbitrary (use initial phase), 1 = Phase align

Bit 2, HO_Usage: 0 = Device Holdover History (DHH) is used; 1 = User supplied history is used.

Bit 5, OOP: In manual mode, when the selected active reference is out of the pull-in range, as specified in register **Disqualification_Range**, 0x10, OOP will determine if the reference is to be followed, 0 = Follow, 1 = Don't follow.

Default value: 0

T4_Bandwidth, 0x3a (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x3a	Not used			Bandwidth select				

Sets the T4 loop bandwidth:

0x3a, bits 4 ~ 0	Bandwidth, Hz
0	107
1	50
2	24
3	12
4	5.9
5	2.9
6	1.5
7	.73
8	0.37
9	0.18
10	0.09
31 ~ 11	Reserved

Default value: 0

T4_Auto_Active_Ref, 0x3b (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x3b	Not used				Selection			

Indicates the automatically selected active reference for T4. (Data valid in automatic mode only)

Bit 3 ~ Bit 0	Selection
0	Freerun
1 ~ 12	Sync with Ref 1 ~ Ref 12
13	Holdover
14, 15	Reserved

T4_Manual_Active_Ref, 0x3c (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x3c	Not used				Selection			

Selects the active reference for T4 in manual reference select mode. Default value: 0

Bit 3 ~ Bit 0	Selection
0	Freerun
1 ~ 12	Sync with Ref 1 ~ Ref 12
13	Holdover
14	Reserved
15	Lock on T0 output

T4_Device_Holdover_History, 0x3d (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x3d	Bits 0 - 7 of 32 bit Device Holdover History							
0x3e	Bits 8 - 15 of 32 bit Device Holdover History							
0x3f	Bits 16 - 23 of 32 bit Device Holdover History							
0x40	Bits 24 - 31 of 32 bit Device Holdover History							

Device holdover history for T4 relative to MCLK. 2's complement. Resolution is 0.745×10^{-3}ppb.
Default value: 0

T4_Long_Term_Accu_History, 0x41 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x41	Bits 0 - 7 of 32 bit Long Term History							
0x42	Bits 8 - 15 of 32 bit Long Term History							
0x43	Bits 16 - 23 of 32 bit Long Term History							
0x44	Bits 24 - 31 of 32 bit Long Term History							

Long term accumulated history for T4 relative to MCLK. 2's complement. Resolution is 0.745×10^{-3} ppb.

T4_Short_Term_Accu_History, 0x45 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x45	Bits 0 - 7 of 32 bit Short Term History							
0x46	Bits 8 - 15 of 32 bit Short Term History							
0x47	Bits 16 - 23 of 32 bit Short Term History							
0x48	Bits 24 - 31 of 32 bit Short Term History							

Short term accumulated history for T4 relative to MCLK. 2's complement. Resolution is 0.745×10^{-3} ppb.

T4_User_Accu_History, 0x49 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x49	Bits 0 - 7 of 32 bit User Holdover History							
0x4a	Bits 8 - 15 of 32 bit User Holdover History							
0x4b	Bits 16 - 23 of 32 bit User Holdover History							

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x4c	Bits 24 - 31 of 32 bit User Holdover History							

User accumulated history for T4 relative to MCLK. 2's complement. Resolution is 0.745×10^{-3} ppb.
Default value: 0.

T4_History_Ramp, 0x4d (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x4d	Not used	Long Term History bandwidth			Short Term History band-width		Ramp control	

Holdover bandwidth and ramp controls for T4:

0x4d, bits 6 ~ 4	Long Term History -3dB Bandwidth
000	9.7 mHz
001	4.9 mHz
010	2.4 mHz
011	1.2 mHz
100	0.61 mHz
101	0.30 mHz

0x4d, bits 3 ~ 2	Short Term History -3dB Bandwidth
00	2.5 Hz
01	1.24 Hz
10	0.62 Hz
11	0.31 Hz

0x4d, bits 1 ~ 0	Ramp control
00	No Control
01	1 ppm/s
10	1.5 ppm/s
11	2 ppm/s

Default value: 0x27 (2.4mHz; 1.24Hz; 2ppm/s)

T4_Priority_Table, 0x4e (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x4e	Ref 2 Priority				Ref 1 Priority			
0x4f	Ref 4 Priority				Ref 3 Priority			
0x50	Ref 6 Priority				Ref 5 Priority			
0x51	Ref 8 Priority				Ref 7 Priority			
0x52	Ref 10 Priority				Ref 9 Priority			
0x53	Ref 12 Priority				Ref 11 Priority			

Reference priority for automatic reference selection mode. Lower values have higher priority:

0x4e - 0x53, 4 bits	Reference Priority
0000	Disable reference
0001 ~ 1111	1 ~ 15

Default value: 0

T4_PLL_Status, 0x54 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x54	HHA 1=Available 0=Not available	AHR 1=Ready 0=Not ready	Reserved	SAP 1=Stop at pull-in range 0=Follow-ing	OOP 1=Out of pull-in range 0=In range	LOL 0=No LOL 1=LOL	LOS 0=No LOS 1=LOS	SYNC: 0=No Sync 1=Sync

SYNC: Indicates synchronization has been achieved
LOS: Loss of signal of the active reference
LOL: Loss of lock (Failure to achieve or maintain lock)
OOP: Out of pull-in range
AHR: Active Holdover History Ready
HHA: Holdover History Available
SAP: Indicates the output clocks stop following the selected reference, caused by out of pull-in range

HHA	AHR	Holdover Status
1	1	Holdover History available: Device Holdover History tracking on the current active reference
1	0	Holdover History available: Device Holdover History based on last available history
0	0	Holdover History not available
0	1	Not applicable

T4_Accu_Flush, 0x55 (W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x55	Not used							HO flush

Writing to this register will perform a flush of the accumulated history. The value of bit zero determines which histories are flushed. Bit 0 = 0, Flush and reset T4 long term history only; bit 0 = 1, flush/reset both T4 long term history and the T4 device holdover history.

CLK0_Sel, 0x56 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x56	Not used						CLK0 Select	

Selects or disables the CLK0 output.
Default value: 0

0x56, bits 1 ~ 0	CLK0 output
0	Disabled
1	155.52MHz
2	125MHz
3	Reserved

CLK1_Sel, 0x57 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x57	Not used					CLK1 Select		

Selects or disables the CLK1 output.

0x57, bits 2 ~ 0	CLK1 output
0	Disabled
1	19.44MHz
2	38.88MHz
3	77.76MHz
4	51.84MHz
5	25MHz
6	50MHz
7	125MHz

Default value: 1

CLK2_Sel, 0x58 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x58	Not used					CLK2 Select		

Selects or disables the CLK2 output.

0x58, bits 1 ~ 0	CLK2 output
0	Disabled
1	19.44MHz
2	38.88MHz
3	77.76MHz
4	51.84MHz
5	25MHz
6	50MHz
7	125MHz

Default value: 2

CLK3_Sel, 0x59 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x59	Not used		CLK3 Select					

Selects or disables the CLK3 output, and sets the pulse width. In variable pulse width, the width may be selected from 1 to 62 times the period of the 155.52MHz output (~6.43ns to 399ns).

0x59, bits 5 ~ 0	CLK3 8kHz output
0	Disabled
1 ~ 62	Pulse width 1 to 62 cycles of 155.52MHz
63	50% duty cycle

Default value: 63

CLK4_Sel, 0x5a (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x5a	Not used		CLK4 Select					

Selects or disables the CLK4 output, and sets the pulse width. In variable pulse width, the width may be selected from 1 to 62 times the period of the 155.52MHz output (~6.43ns to 399ns).

0x5a, bits 5 ~ 0	CLK4 2kHz output
0	Disabled
1 ~ 62	Pulse width 1 to 62 cycles of 155.52MHz
63	50% duty cycle

Default value: 63

CLK5_Sel, 0x5b (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x5b	Not used						CLK5 Select	

Selects or disables the CLK5 output.

0x5b, bits 1 ~ 0	CLK5 output
0	Disabled
1	44.736MHz (DS3)
2	34.368MHz (E3)
3	Reserved

Default value: 2

CLK6_Sel, 0x5c (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x5c	Not used				CLK6 Select			

Selects or disables the CLK6 output.

0x5c, bits 3 ~ 0	CLK6 output
0	Disabled
1	2.048MHz
2	4.096MHz

0x5c, bits 3 ~ 0	CLK6 output
3	8.192MHz
4	16.384MHz
5	32.768MHz
6, 7, 8	Reserved
9	1.544MHz
10	3.088MHz
11	6.176MHz
12	12.352MHz
13	24.704MHz
14, 15	Reserved

Default value: 1

CLK7_Sel, 0x5d (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x5d	Not used						CLK7 Select	

Selects or disables the CLK7 output.

0x5d, bits 1 ~ 0	CLK7 output
0	Disabled
1	1.544MHz (T1)
2	2.048MHz (E1)
3	Reserved

Default value: 2

Intr_Event, 0x5e (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x5e	Event 7: T4 cross reference changed from non-active to active	Event 6: T4 cross reference changed from active to non-active	Event 5: T4 DPLL status changed	Event 4: T4 active reference changed in auto selection mode	Event 3: T0 cross reference changed from non-active to active	Event 2: T0 cross reference changed from active to non-active	Event 1: T0 DPLL status changed	Event 0: T0 active reference changed in auto selection mode
0x5f							Event 9: Any reference changed from disqualified to qualified	Event 8: Any reference changed from qualified to disqualified

Interrupt event, 0 = no event, 1 = event occurred. Interrupt 8 and 9 apply to the 12 reference inputs only. Interrupts are cleared by writing “1’s” to the bit positions to be cleared (See **General Register Operation, Clearing bits in the Interrupt Status Register** section).

Intr_Enable, 0x60 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x60	Intr 7 Enable	Intr 6 Enable	Intr 5 Enable	Intr 4 Enable	Intr 3 Enable	Intr 2 Enable	Intr 1 Enable	Intr 0 Enable
0x61							Intr 9 Enable	Intr 8 Enable

Interrupt disable/enable, 0 = disable, 1 = enable.
Default value: 0

Performance

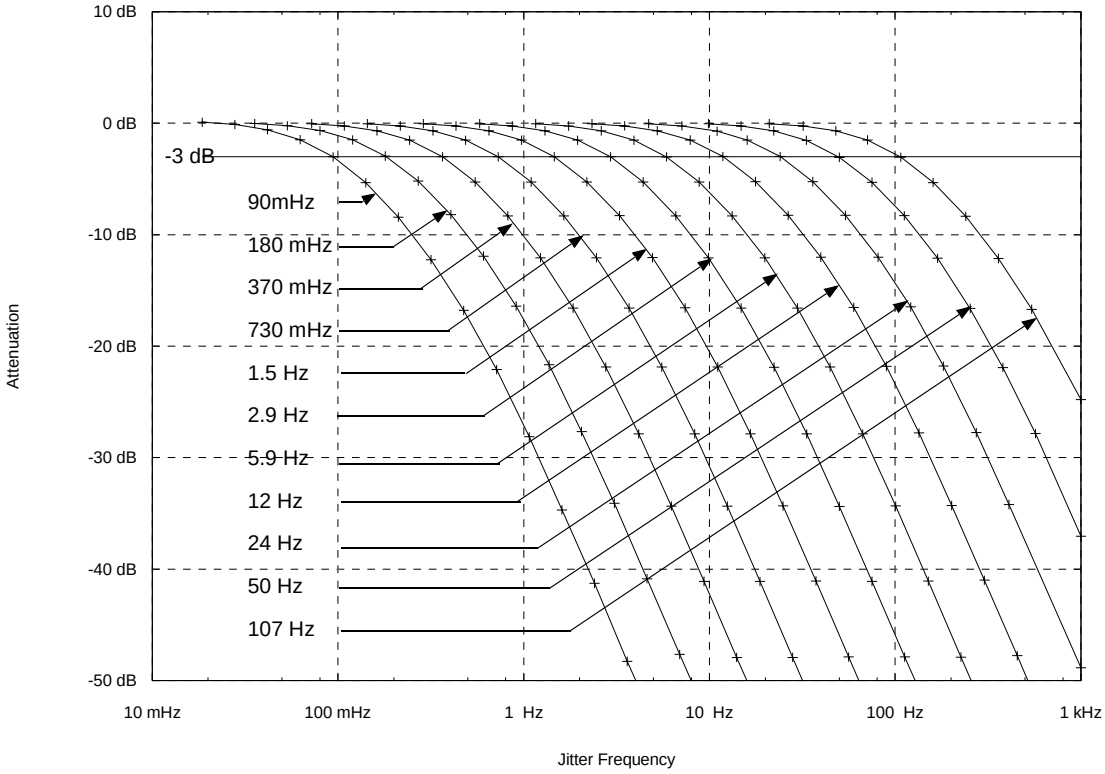


Figure 17: Jitter Attenuation

Application Notes

This section describes typical application use of the STC5130 device. The General section applies to all application variations.

General

Power and Ground

Well-planned noise-minimizing power and ground are essential to achieving the best performance of the device. The device requires 3.3 and 1.8V digital power and 1.8V analog power input. All digital I/O is at 3.3V, LVTTL compatible.

It is desirable to provide individual 0.1uF bypass capacitors, located close to the chip, for each of the power input leads, subject to board space and layout constraints. On power-up, it is desirable to have the 3.3V either lead or be coincident with, but not lag the application of both 1.8V supplies.

Digital ground should be provided by as continuous a ground plane as possible.

Note: Un-used reference inputs must be grounded.

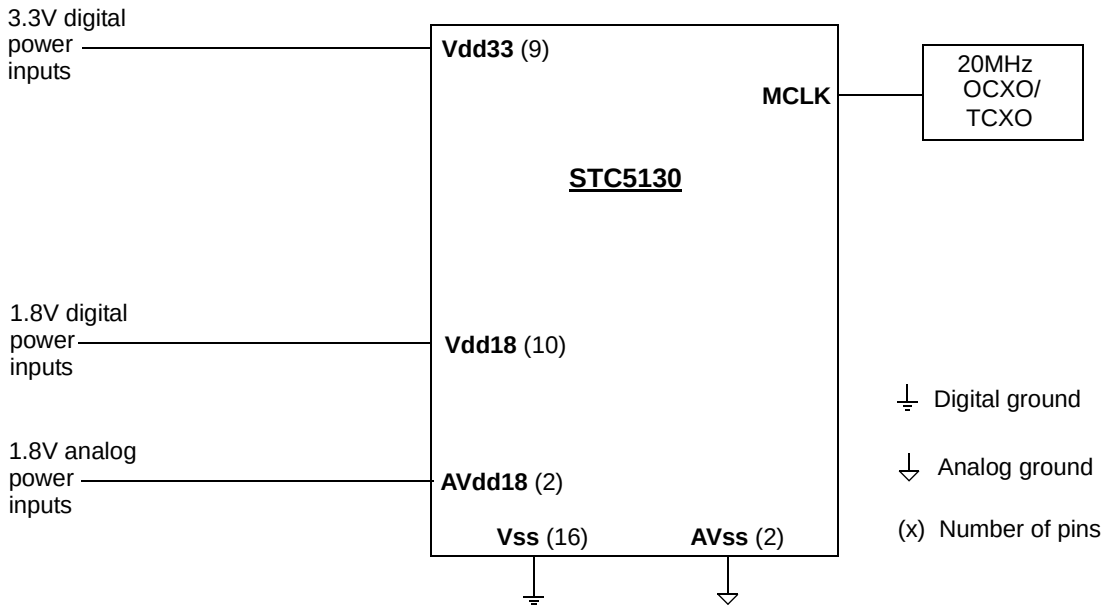
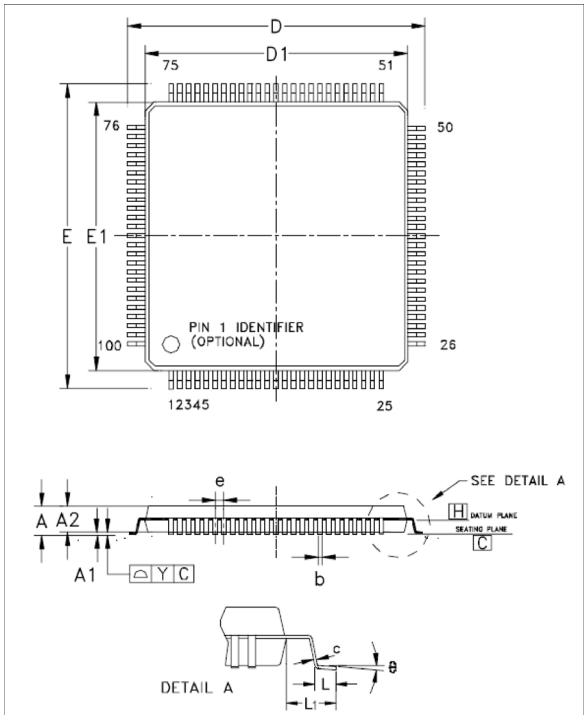


Figure 18: Power, Ground and Oscillator connections

The external 20MHz TCXO/OCXO master oscillator is connected to the **MCLK** pin.

Mechanical Specifications



Symbol	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.09		0.20	0.004		0.008
D		16.00	BSC		0.630	
E		16.00	BSC		0.630	
e		0.50	BSC		0.020	
D1		14.00	BSC		0.551	
E1		14.00	BSC		0.551	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00	REF		0.039	
Y		0.08			0.003	
θ	0°	3.5°	7°	0°	3.5°	7°

Controlling dimensions are in millimeters

Ordering Information

Part Number	Description
STC5130	Commercial Temperature Range Model
STC5130-I	Industrial Temperature Range Model

Revision History

The following table summarizes significant changes made in each revision. Additions reference current pages.

Revision	Change Description	Pages
P01	Initial issue	

For more information, contact:

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