STC5170
Synchronous Clock for SETS
Data Sheet

Description

The STC5170 is an integrated single chip solution for the synchronous clock in SDH, SONET, and Synchronous Ethernet network elements. The device is fully compliant with ITU-T G.813, and Telcordia GR1244, and GR253.

The STC5170 accepts 2 reference inputs and generates 2 independent synchronized output clocks. Reference input frequencies are automatically detected. All reference switches are hitless. Synchronized outputs may be programmed for a wide variety of SONET and SDH as well as Synchronous Ethernet frequencies.

The clock generator includes a DPLL (Digital Phase-Locked Loop), which may operate in the Freerun, Synchronized, and Holdover modes.

A standard SPI bus provide access to the STC5170's internal control and status registers. The device operates with an external 20MHz OCXO or TCXO as its MCLK.

Features

- For SDH SETS
- For Synchronous Ethernet
- For SONET Stratum 4E and 4
- Complies with ITU-T G.813, Telcordia GR1244, and GR253
- Accepts 2 clock reference inputs
- Reference clock inputs are automatically frequency detected
- Supports manual reference selection (via pin control)
- 2 synchronized output clocks
- Hit-less reference switching
- Phase rebuild on re-lock and reference switches
- Better than 0.1 ppb holdover accuracy
- Programmable loop bandwidth, from 1.5Hz to 107Hz
- Supports SPI bus interface
- IEEE 1149.1 JTAG boundary scan
- Available in TQ100 package

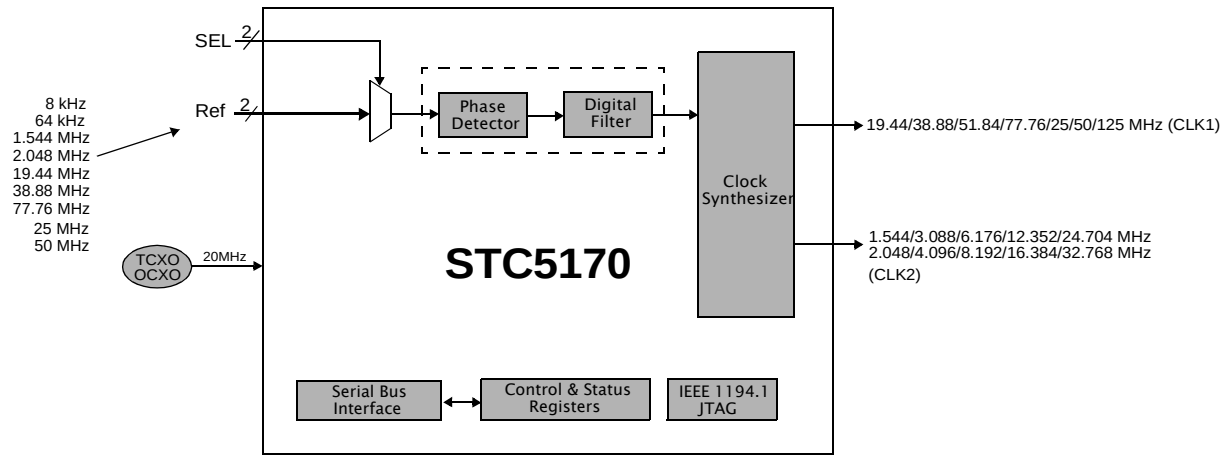

Figure 1: Block Diagram

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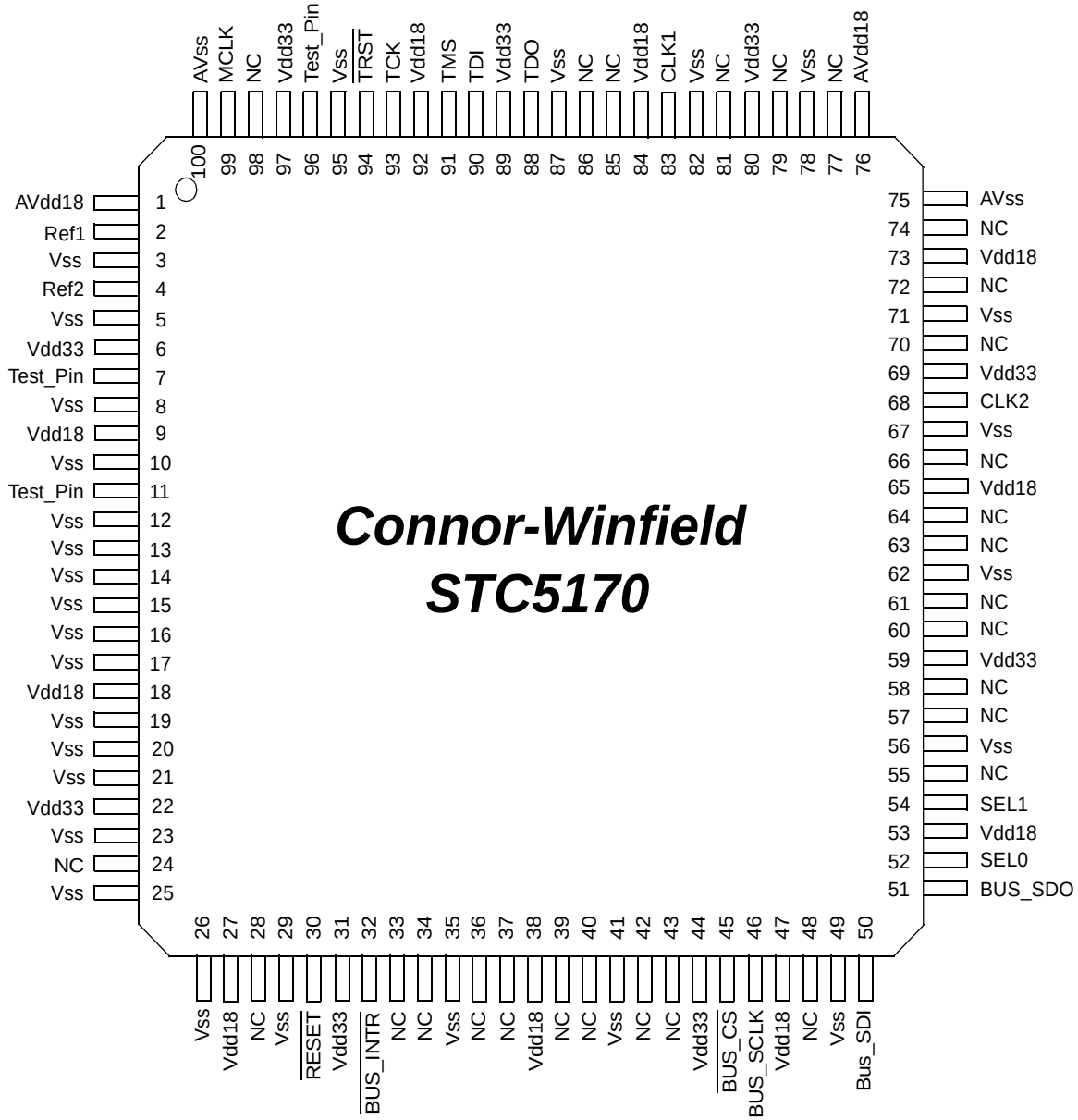
STC5170 Pin Diagram (Top View)



Note: Pins labeled “Test Pin” must be grounded.

STC5170 Pin Description

Table 1: Pin Description

Pin Name	Pin #	I/O	Description
Vdd33	6, 22, 31, 44, 59, 69, 80, 89, 97		3.3V power input
Vdd18	9, 18, 27, 38, 47, 53, 65, 73, 84, 92		1.8V power input
Vss	3, 5. 8, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 25, 26, 29, 35, 41, 49, 56, 62, 67, 71, 78, 82, 87, 95		Digital ground
AVdd18	1, 76		1.8V analog power input
AVss	75,100		Analog ground
$\overline{\text{TRST}}$	94	I	JTAG boundary scan reset, active low
TCK	93	I	JTAG boundary scan clock
TMS	91	I	JTAG boundary scan mode selection
TDI	90	I	JTAG boundary scan data input
TDO	88	O	JTAG boundary scan data output
$\overline{\text{RESET}}$	30	I	Active low to reset the chip
MCLK	99	I	Master clock input, 20MHz
$\overline{\text{BUS\_CS}}$	45	I	SPI Chip select ($\overline{\text{CS}}$)
BUS_SCLK	46	I	SPI clock input (SCLK)
BUS_SDI	50	I	SPI data input (SDI)
BUS_SDO	51	O	SPI data output (SDO)
$\overline{\text{BUS\_INTR}}$	32	O	Interrupt
SEL1	54	I	Select active reference
SEL0	52	I	Select active reference
REF1	2	I	Reference input 1
REF2	4	I	Reference input 2
CLK1	83	O	19.44/38.88/51.84/77.76/25/50/125 MHz

Table 1: Pin Description

Pin Name	Pin #	I/O	Description
CLK2	68	O	1.544/3.088/6.176/12.352/24.704/2.048/4.098/8.192/16.384/32.768 MHz
NC	24, 28, 33, 34, 36, 37, 39, 40, 42, 43, 48, 55, 57, 58, 60, 61, 63, 64, 66, 70, 72, 74, 77, 79, 81, 85, 86. 98		No connection. Pin must be left open.
Test_Pin	7,11,96		Test pin, must be grounded for normal operation

All I/O is LVCMOS.

Absolute Maximum Ratings

Table 2: Absolute Maximum Ratings

Symbol	Parameter	Min.	Max	Units	Notes
Vdd33	Logic power supply voltage, 3.3V	-0.5	4.5	volts	1
Vdd18	Logic power supply voltage, 1.8V	-0.5	2.5	volts	1
AVdd18	Analog power supply voltage, 1.8V	-0.5	2.5	volts	1
VIN	Logic input voltage	-0.5	5.5	volts	1
TSTG	Storage Temperature	-65	150	°C	1

Note 1: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the Recommended Operating Conditions.

Operating Conditions and Electrical Characteristics

Table 3: Recommended Operating Conditions and Electrical Characteristics

Symbol	Parameter	Min.	Nominal	Max.	Units	Notes
Vdd33	3.3V digital power supply voltage	3.0	3.3	3.6	Volts	
Vdd18	1.8V digital power supply voltage	1.65	1.8	1.95	Volts	
AVdd18	1.8V analog power supply voltage	1.65	1.8	1.95	Volts	
VIH (3.3V)		2.0		5.5		2
VIL (3.3V)		-0.3		0.8		2
VOH (3.3V)	High level output voltage (IOH = -12mA)	2.4			Volts	2
VOL (3.3V)	Low level output voltage (IOL =12mA)			0.4	Volts	2
CIN	Input capacitance		8		pF	
TRIP	Input reference signal positive pulse width	10			ns	
TRIN	Input reference signal negative pulse width	10			ns	
TA	Operating Ambient Temperature Range (Commercial)	0		70	°C	
TA	Operating Ambient Temperature Range (Industrial)	-40		85	°C	
Icc (Vcc)	3.3V digital supply current		TBD		mA	
Icc (AVcc)	3.3V analog supply current		TBD		mA	
Pd	Device power dissipation		TBD		W	

Note 2: LVCMOS 3.3 compatible

Register Map

Table 4: Register Map

Addr	Reg Name	Bits	Type	Description
0x00	Chip_ID	15-0	R	Chip ID, 0x5170
0x02	Chip_Rev	7-0	R	Chip revision number
0x03	Chip_Sub_Rev	7-0	R	Chip sub-revision
0x04	Pullin_Range	9-0	R/W	Reference pullin range, 0 ~ 102.3 ppm
0x06	Control_Mode	5	R/W	OOP - Follow/Don't Follow
0x07	Bandwidth	4-0	R/W	Loop bandwidth selection
0x08	Active_Ref	1-0	R	Indicate the reference selection status from pin SEL1 and SEL0
0x09	PLL_Status	7-0	R	OOP, LOL, LOS, Sync, HHA, AHR, SAP
0x0a	CLK1_Sel	2-0	R/W	19.44/38.88/51.84/77.76/25/50/125 MHz or disable select for CLK1
0x0b	CLK2_Sel	3-0	R/W	DS1 x n / E1 x n or disable selector for CLK2
0x0c	Intr_Event	1	R/W	Interrupt event
0x0d	Intr_Enable	1	R/W	Interrupt enable

General Description

The STC5170 is an integrated single chip solution for the synchronous clock in SDH (SETS), SONET, and Synchronous Ethernet network elements. It's highly integrated design implements all of the necessary reference selection, digital filtering, synthesis, and control functions. An external OCXO or TCXO at 20 MHz completes a system level solution (see Functional Block Diagram, Figure 1).

The STC5170 includes one DPLL (Digital Phase-Locked Loop) implementing the timing functions of the clock generator. The user may select one of 2 reference inputs as its active reference. The STC5170 may output 2 synchronous clocks.

The clock generator may operate in Freerun, Synchronized, or Holdover mode. In freerun, the clock outputs are synthesized from the MCLK. The stability of freerun is simply determined by the OCXO/TCXO. In synchronized mode, the chip phase locks to the selected input reference. All reference switches are performed in a hitless manner, and frequency ramp controls ensure smooth output signal transitions. When references are switched, the device will minimize phase transitions in the output clocks. While synchronized, a frequency history is accumulated. In holdover mode, the chip outputs are synthesized according to this history.

The Digital Phase Locked Loop which provides the critical filtering and frequency/phase control functions is implemented with the NOVA kernal - a set of well-proven algorithms and control that meet or exceed all requirements and lead the industry in critical jitter and accuracy performance parameters. The loop bandwidth of the DPLL may be user configured.

Reference frequencies are autodetected and may each be 8kHz, 64kHz, 1.544MHz, 2.048MHz, 19.44MHz, 38.88MHz, 77.76MHz, 25MHz, or 50 MHz.

The device generates 2 independent synchronized output clocks. The first may be programmed at 19.44/38.88/51.84/77.76/25/50/125 MHz. The second is programmable at the frequency of 1, 2, 4, 8, or 16 x T1 or E1.

Reference selection is under the control of chip pin inputs. The remaining control functions are provided via a standard SPI serial bus interface. This provides access to the STC5170's simple to use internal control and status registers.

Detailed Description

Chip Master Clock Input

The device operates with an external 20MHz OCXO or TCXO as its master clock, connected to the **MCLK** input, pin 99.

Digital Phase Locked Loop

The STC5170 clock generator has a DPLL, including a phase detector and a digital filter.

The DPLL may select the REF1 or REF2 reference clock as the synchronization source.

Reference Inputs

The 2 external reference inputs may each be at 8kHz, 64kHz, 1.544MHz, 2.048MHz, 19.44MHz, 38.88MHz, 77.76MHz, 25MHz, or 50MHz. Input frequencies are detected automatically.

The selected active reference is monitored for activity and frequency offset. Loss of activity will set the LOS bit and frequency offset beyond the pull-in range sets the OOP bit in the **PLL_Status** register (0x09). The pull-in range is set by writing to the **Pullin_Range** register (0x04).

Active Reference and Operating Mode Selection

The reference and DPLL operating mode are selected with the **SEL(1,0)** pins, as shown below. Their state may be read back from the **Active_Ref** (0x08) register.

SEL1	SEL0	Selection
0	0	Freerun
0	1	Sync on Ref 1
1	0	Sync on Ref 2
1	1	Holdover

Digital Phase Locked Loop General Description

The clock generator of the STC5170 has a DPLL, including a phase detector and a digital filter.

The clock generator may select one of the two input reference clocks and operate in the Freerun, Synchronized, or Holdover mode. The transfer into and out of holdover or freerun mode is designed to be smooth and free of hits:

1. Free Run
In freerun mode, the **CLK(1,2)** clock outputs are synthesized from MCLK and have the stability of the external TCXO/OCXO. The transfer into and out of freerun mode is designed to be smooth and free of hits.

2. Synchronized
The **CLK(1,2)** clock outputs are phase locked to and track the selected input reference. Once satisfactory lock is achieved, the “synchronized” state is entered, and the “SYNC” bit is set in the **DPLL_Status** register (0x09).

The user may configure the loop bandwidth of the DPLL. The DPLL loop bandwidth is selectable from 1.5Hz to 107Hz, by writing to the **Bandwidth** register (0x07).

3. Holdover
Upon entering holdover mode, the **CLK(1,2)** clock outputs are determined from the holdover history established. The internally accumulated holdover history is a weighted average, with a single-pole low pass filtering algorithm applied. The -3dB point of the filtering algorithm is fixed at 2.4mHz. Output clock accuracy in holdover mode is therefore effectively determined by MCLK (the external TCXO/OCXO) stability. The transfer into and out of holdover mode is designed to be smooth and free of hits.

DPLL Operating Mode Details

The clock generators may operate in the Freerun, Synchronized, or Holdover modes, including some variants thereof:

Freerun Mode
In freerun mode, the **CLK(1,2)** clock outputs are syhthesized and have the stability of MCLK (the external TCXO/OCXO). Freerun mode may be entered by the appropriate selection of the **SEL(1,0)** pins.

On all transitions into freerun or back from freerun, a maximum slew rate of 2 ppm/second is applied to ensure the transition to be smooth and free of hits.

Synchronized Mode

The Synchronized mode may be entered by the appropriate selection of the **SEL(1,0)** pins.

User may configure the DPLL's loop bandwidth. The loop bandwidth is selectable from 1.5Hz to 107Hz by writing to the **Bandwidth** register (0x07).

When reference switching, a phase relationship relative to the reference input will be rebuilt. The DPLL will be in frequency locking stage intially. When the synrhonization achieved ("SYNC" bit will be asserted), the phase error will be rebuilt, arbitrary to the phase of the input reference.

There are two special cases of the Synchronized mode:

a) "Zombie" Mode – If the selected active reference signal is lost, the DPLL output is generated according to a short-term history.

b) Out of Pull-in Range Mode - If the selected reference exceeds the pull-in range as programmed by the application in the **Pullin_Range** register (0x04), the DPLL output may be programmed to stay at the pull-in range limit, or to follow the reference. This is programmed by writing to "OOP" bit of the **Control_Mode** register (0x06), specifying whether to follow or not follow a reference that has exceded the pull-in range.

When the device has locked on a reference, the "SYNC" bit 0 is set in the **DPLL_Status** register (0x09). If there is a failure to achieve or maintain lock, the "LOL" bit is set in the **DPLL_Status** register.

Holdover Mode

Holdover mode is analogous to the Freerun mode, except the "frequency offset" is supplied from the holdover history. The device uses the internal accumulated holdover history to synthesize the output clocks in holdover mode.

Three holdover histories are built:

1) **Short-Term History** – The short-term average frequency of the clock outputs. The weighted single-pole low-pass filter has a fixed -3dB point of 1.24 Hz. The short-term history is used in the event of an active reference loss.
2) **Long-Term History –** The long-term average frequency of the clock outputs, while synchronized to a selected external reference. The weighted single-pole low-pass filter has a fixed -3dB point 2.4 mHz. Internally, an express mode is used after reset by applying a lower time constant for 15 minutes to speed up the history accumulation process. This accumulation process will be reset whenever the selected reference is switched or loss of lock occurs. The accumulation process will then resume after the "SYNC" bit is asserted in the **DPLL_Status** register (0x09).
3) **Device Holdover History** – This history determines the **CLK(1,2)** clock outputs when entering holdover mode. The initial history is zero offset, equal to MCLK. This history will begin to be updated by the long term history after the 15 minute express mode time has completed. Updating will stop if the long term history accumulation process is reset as a result of a reference switch or loss of lock. Thus, the previous holdover history will persist until a new long term history is accumulated following a reference switch or the attendant re-building of the long term history after loss of lock. The "AHR" bit of the **DPLL_Status** register (0x09) is set to "1" during updating, but will revert to "0" when updating stops.

The "HHA" bit of the **DPLL_Status** register (0x09) is asserted "1", indicating the availability of the device holdover history, when the history has been first updated from the long term history.

On all transitions into holdover or back from holdover, a maximum slew rate of 2 ppm/second is applied to ensure the transition to be smooth and free of hits.

Output Clocks

The clock output section includes 2 clock generators, an APLL, two dividers, and generates 2 synchronized clocks, as shown in figure 2.

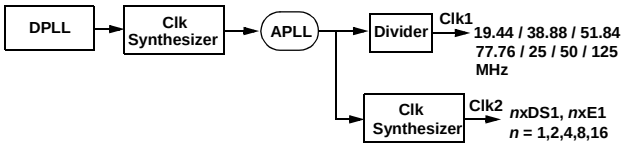


Figure 2: Output Clocks

The first synthesizer drives an analog PLL and generates **CLK1**:

- **CLK1**: Programmable at 19.44MHz, 38.88MHz, 51.84MHz, 77.76, 25,50 MHz, and “disabled”, by writing to the **CLK1_Sel** register (0x0a), bits 0 - 2.

The second synthesizer generates **CLK2**:

- **CLK2**: Programmable at nxDS1 or nxE1 rate, where n=1,2,4,8,16, or may be disabled, by writing to the **CLK2_Sel** register (0x0b), bits 0 - 3.

When a clock output is disabled, the pin is tri-stated.

Processor Interface Descriptions

The STC5170 supports the SPI bus interface:

SPI Bus Mode

The SPI interface bus mode uses the $\overline{\text{BUS\_CS}}$, BUS_SCLK, BUS_SDI, and BUS_SDO respectively, with timing as shown in figures 3 and 4:

Serial Bus Timing

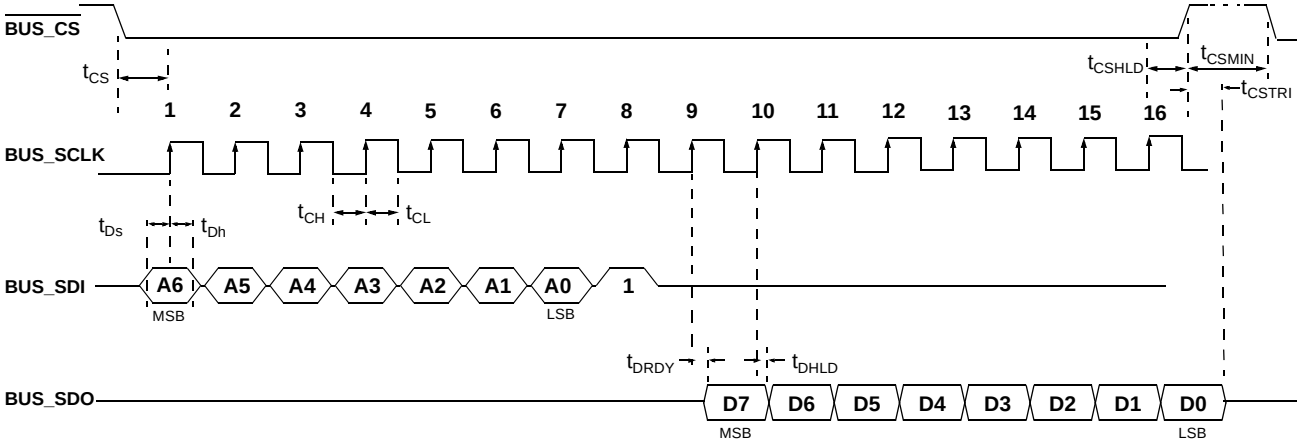


Figure 3: Serial Bus Timing, Read access

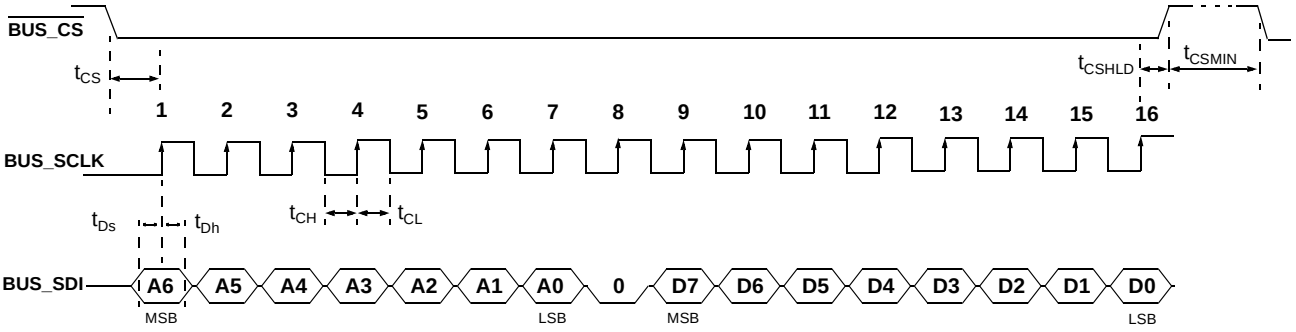


Figure 4: Serial Bus Timing, Write access

Table 5: Serial Bus Timing

Symbol	Description	Min	Max	Unit
t_{CS}	$\overline{\text{BUS\_CS}}$ low to BUS_SCLK high	10		ns
t_{CH}	BUS_CLK high time	25		ns
t_{CL}	BUS_SCLK low time	25		ns
t_{Ds}	Data setup time	10		ns
t_{Dh}	Data hold time	10		ns
t_{DRDY}	Data ready		7	ns
t_{DHLD}	Data hold	3		ns
t_{CSHLD}	Chip select hold	30		ns
t_{CSTRI}	Chip select to data tri-state		5	ns
t_{CSMIN}	Minimum delay between successive accesses	50		ns

Register Descriptions and Operation

General Register Operation

The STC5170 device has 1, and 2 byte registers. One byte registers are read and written directly. Two byte registers must be read and written in a specific manner and order, as follows:

Two byte register reads

A two byte register read must commence with a read of the least significant byte first. This triggers a transfer of the second byte to a holding resgister, ensuring that the remaining data will not change with the continuing operation of the device. The remaining byte may then be read (must be read consecutively with no intervening read/writes from/to other registers).

Two byte register writes

A two byte register write must commence with a write to the least significant byte first. Two byte register writes are temporarily stored in a holding register, and are transferred to the target register when the most significant byte is written. The second byte must be written consecutively, with no intervening read/writes from/to other registers.

Clearing bits in the Interrupt Status Register

Interrupt event register (**Intr_Event**, 0x0c) bits are cleared by writing a “1” to the bit position to be cleared. Interrupt bit positions to be left as is are written with a “0”.

Chip_ID, 0x00 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x00	0x71							
0x01	0x51							

Chip_Rev, 0x02 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x02	Revision Number							

Chip_Sub_Rev, 0x03 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x03	Sub-Revision Number							

Pullin_Range, 0x04 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x04	Lower 8 bits							
0x05	Not used						Upper 2 bits	

Reference pull-in range, from 0 to +102.3 ppm, in 0.1 ppm steps. (See **Control_Mode** register).
Default value: 110

Control_Mode, 0x06 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x06	Not used		OOP: Out of Pull-in range: 0=Follow 1=Don't follow	Not used				

DPLL mode control.

Bit 5, OOP: When the selected active reference is out of the pull-in range, as specified in register **Pullin_Range**, 0x04, OOP will determine if the reference is to be followed, 0 = Follow, 1 = Don't follow.
Default value: 0

Bandwidth, 0x07 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x07	Not used			Bandwidth select				

Sets the loop bandwidth. Default value: 6

0x07, bits 4 ~ 0	Bandwidth, Hz
0	107
1	50
2	24
3	12
4	5.9
5	2.9
6	1.5
31 ~ 7	Reserved

Active_Ref, 0x08 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x08	Not used						SEL[1:0] pin state	

Indicates the state of the **SEL(1/0)** pins. Bit 1 corresponds to **SEL1**, Bit 0 corresponds to **SEL0**.

PLL_Status, 0x09 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x09	HHA 1=Available 0=Not available	AHR 1=Ready 0=Not ready	Reserved	SAP 1=Stop at pull-in range 0=Follow-ing	OOP 1=Out of pull-in range 0=In range	LOL 0=No LOL 1=LOL	LOS 0=No LOS 1=LOS	SYNC: 0=No Sync 1=Sync

SYNC: Indicates synchronization has been achieved
LOS: Loss of signal of the active reference
LOL: Loss of lock
OOP: Out of pull-in range
AHR: Active Holdover History Ready
HHA: Holdover History Available
SAP: Indicates the output clocks stop following the selected reference, caused by out of pull-in range

HHA	AHR	Holdover Status
1	1	Holdover History available: Device Holdover History tracking on the current active reference
1	0	Holdover History available: Device Holdover History based on last available history
0	0	Holdover History not available
0	1	Not applicable

CLK1_Sel, 0x0a (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0a	Not used					CLK1 Select		

Selects or disables the CLK1 output. Disabled output is tri-state.

0x0a, bits 2 ~ 0	CLK1 output
0	Disabled
1	19.44MHz
2	38.88MHz
3	77.76MHz
4	51.84MHz
5	25MHz
6	50MHz
7	Disabled

Default value: 1

CLK2_Sel, 0x0b (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0b	Not used				CLK2 Select			

Selects or disables the CLK2 output. Disabled output is tri-state.
Default = 1, 2.048MHz:

0x0b, bits 3 ~ 0	CLK3 output
0	Disabled
1	2.048MHz
2	4.096MHz
3	8.192MHz
4	16.384MHz
5	32.768MHz
6, 7, 8	Reserved
9	1.544MHz
10	3.088MHz
11	6.176MHz
12	12.352Hz
13	24.704MHz
14, 15	Reserved

Intr_Event, 0x0c (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0c	Not used						Event 1: DPLL status changed	Not used

Interrupt event, 0 = no event, 1 = event occurred. Interrupts are cleared by writing “1’s” to the bit positions to be cleared (See **General Register Operation, Clearing bits in the Interrupt Status Register** section).

Intr_Enable, 0x0d (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0d	Not used						Intr 1 Enable	Not used

Interrupt disable/enable, 0 = disable, 1 = enable.
Default value: 0

Application Notes

General

Power and Ground

Well-planned noise-minimizing power and ground are essential to achieving the best performance of the device. The device requires 3.3 and 1.8V digital power and 1.8V analog power input. All digital I/O is at 3.3V, LVTTL compatible.

It is desirable to provide individual 0.1uF bypass capacitors, located close to the chip, for each of the power input leads, subject to board space and layout constraints. On power-up, it is desirable to have the 3.3V either lead or be coincident with, but not lag the application of both 1.8V supplies.

Digital ground should be provided by as continuous a ground plane as possible.

Note: Un-used reference inputs must be grounded.

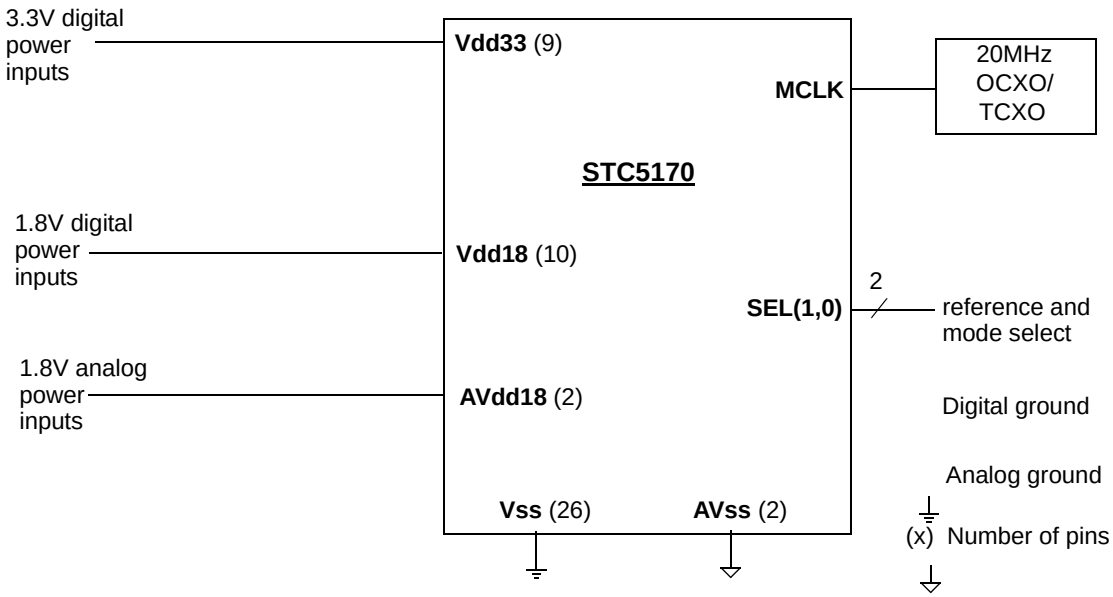


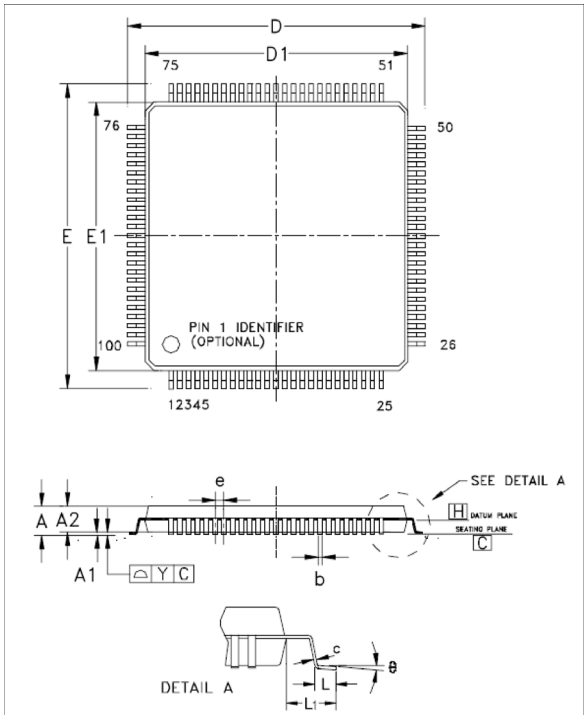
Figure 5: Power, Ground, Oscillator and Control connections

The external 20MHz TCXO/OCXO master oscillator is connected to the **MCLK** pin.

SEL(1,0) select the PLL references and operating modes, as shown below:

SEL1	SEL0	Selection
0	0	Freerun
0	1	Sync on Ref 1
1	0	Sync on Ref 2
1	1	Holdover

Mechanical Specifications



Symbol	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.09		0.20	0.004		0.008
D		16.00	BSC		0.630	
E		16.00	BSC		0.630	
e		0.50	BSC		0.020	
D1		14.00	BSC		0.551	
E1		14.00	BSC		0.551	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00	REF		0.039	
Y		0.08			0.003	
θ	0°	3.5°	7°	0°	3.5°	7°

Contolling dimensions are in millimeters

Revision History

The following table summarizes significant changes made in each revision. Additions reference current pages.

Revision	Change Description	Pages
P01	Initial issue	

For more information, contact:

2111 Comprehensive DR
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