STC5420
Synchronous Clock for SETS
Data sheet

Description

The RoHS 6/6 compliant STC5420 is a single chip clock synchronization solution for applications in SDH/SETS, SONET, and Synchronous Ethernet network elements. The device is fully compliant with ITU-T G.813 option 1 and 2, G.8262 EEC Opt1 and Opt2 and Telcordia GR1244 and GR253.

The STC5420 accepts 12 clock reference inputs and generates 10 synchronized clock outputs: CLK1~CLK8, frame pulse clock CLK8K at 8kHz, and frame pulse clock CLK2K at 2kHz. CLK1~CLK8 may be programmed for wide variety of frequencies from 1MHz up to 156.25MHz, in 1kHz steps. Reference inputs are individually monitored for activity and quality. Reference selection may be automatic, manual, and hard-wired manual.

Two independent timing generators, T0 and T4, may operate in the ***Freerun***, ***Synchronized***, ***Pseudo Holdover***, and ***Holdover*** mode. Each timing generator includes a DSP-based PLL. Synchronized mode external timing while freerun and holdover mode are self-timing. T0 supports Master/Slave and Multiple Master operation for redundant design. T4 only supports master operation. DSP-based PLL technology removes any external component except the oscillator. It provides excellent performance and reliability to STC5420.

The STC5420 is clocked by an external oscillator (TCXO or OCXO). Using a well-chosen external oscillator ensures the STC5420 meet the required specification and standards.

Features

- Complies with ITU-T G.813 Opt1/Opt2, G.8262 EEC Opt1/Opt2, Telcordia GR1244 and GR253 (Stratum3/4E/4/SMC)
- Two timing generators T0 and T4; T4 may lock to T0's synchronized output
- Supports Master/Slave and Multiple-Master redundant application (T0 timing generator only)
- Provides programmable compensation for phase delay between master and slave unit, in 0.1ns steps
- Accepts external oscillator at frequency of 10MHz, 12.8MHz, 19.2MHz,or 20MHz with programming
- Accepts 12 clock reference inputs
- Supports frequency auto detection or manually acceptable frequency for reference inputs. Each of them is monitored for activity and quality
- Automatic/manual/hard-wired manual reference select
- Outputs 10 synchronized clock outputs, including 2 frame pulse clocks CLK8K and CLK2K
- 10 clock synthesizers generate frequencies
- Programmable phase skew in synthesizer level
- Phase-align or hit-less reference locking/switching
- Programmable loop bandwidth, from 0.1Hz to 100Hz
- Supports bus interface: Intel, Motorola, Multiplex, SPI
- Single 3.3V operation
- IEEE 1149.1 JTAG boundary scan
- Available in TQFP100 package

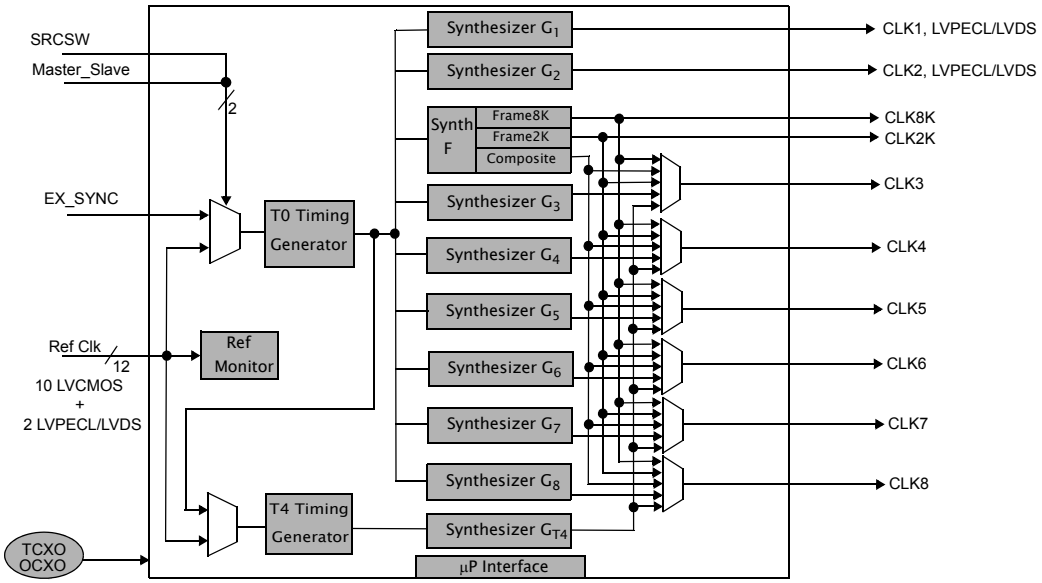

Figure 1:Functional Block Diagram

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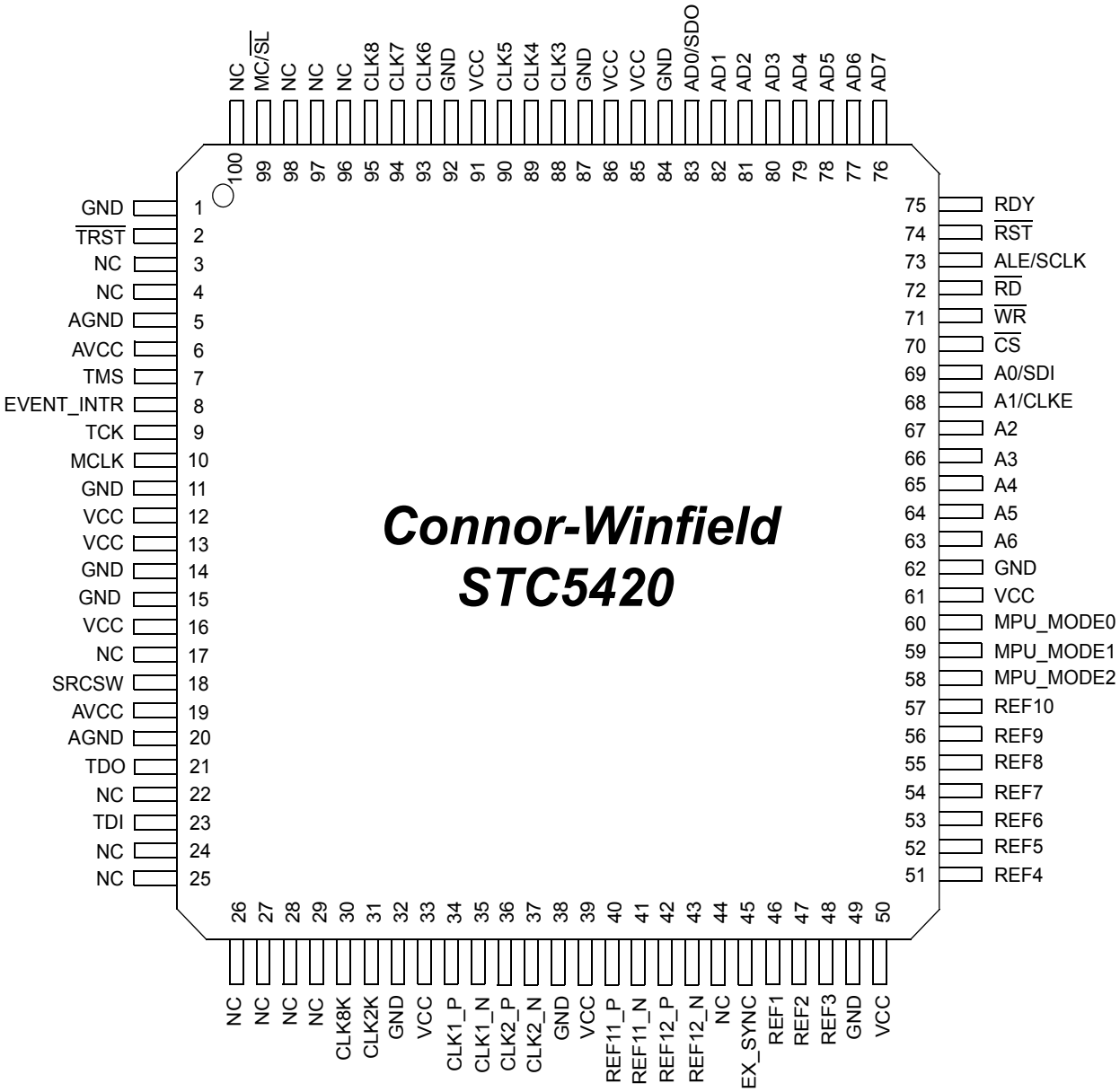


STC5420 Pin Description

All I/O is LVCMOS, except for CLK1 and CLK2 are LVPECL/LVDS. REF11 and REF12 are LVPECL/LVDS.

Table 1: Pin Description

Pin Name	Pin #	I/O	Description
AVCC	6,19,		3.3V analog power input
AGND	5, 20		Analog ground
VCC	12, 13, 16, 33, 39, 50, 61, 85, 86, 91		3.3V digital power input
GND	1, 11, 14, 15, 32, 38, 49, 62, 84, 87, 92		Digital ground
$\overline{\text{TRST}}$	2	I	JTAG boundary scan reset, active low
TCK	9	I	JTAG boundary scan clock
TMS	7	I	JTAG boundary scan mode selection
TDI	23	I	JTAG boundary scan data input
TDO	21	O	JTAG boundary scan data output
$\overline{\text{RST}}$	74	I	Active low to reset the chip
MCLK	10	I	Master clock input (TCXO or OCXO)
EVENT_INTR	8	O	Event interrupt
MC/$\overline{\text{SL}}$	99	I	Select master or slave mode for T0
EX_SYNC	45	I	Frame Sync signal
REF1	46	I	Reference input 1
REF2	47	I	Reference input 2
REF3	48	I	Reference input 3
REF4	51	I	Reference input 4
REF5	52	I	Reference input 5
REF6	53	I	Reference input 6
REF7	54	I	Reference input 7
REF8	55	I	Reference input 8
REF9	56	I	Reference input 9
REF10	57	I	Reference input 10
REF11_P	40	I	Differential reference input 11 positive(LVPECL/LVDS)
REF11_N	41	I	Differential reference input 11 negative(LVPECL/LVDS)
REF12_P	42	I	Differential reference input 12 positive(LVPECL/LVDS)

Table 1: Pin Description

Pin Name	Pin #	I/O	Description
REF12_N	43	I	Differential reference input 12 negative(LVPECL/LVDS)
CLK1_P	34	O	Clock output CLK1 positive. 1MHz to 156.25MHz, in 1kHz steps, from Synthesizer G_1 LVPECL or LVDS
CLK1_N	35	O	Clock output CLK1 negative, 1MHz to 156.25MHz, in 1kHz steps, from Synthesizer G_1 LVPECL or LVDS
CLK2_P	36	O	Clock output CLK2 positive. 1MHz to 156.25MHz, in 1kHz steps, from Synthesizer G_2 LVPECL or LVDS
CLK2_N	37	O	Clock output CLK2 negative. 1MHz to 156.25MHz, in 1kHz steps, from Synthesizer G_2 LVPECL or LVDS
CLK3	88	O	Clock output CLK3. 1MHz to 156.25MHz, in 1kHz steps, from Synthesizer G_3 or Synthesizer G_{T4} (T4); 2kHz, 8kHz or proprietary composite signal from Synthesizer F. LVCMOS.
CLK4	89	O	Clock output CLK4. 1MHz to 156.25MHz, in 1kHz steps, from Synthesizer G_4 or Synthesizer G_{T4} (T4); 2kHz, 8kHz or proprietary composite signal from Synthesizer F. LVCMOS.
CLK5	90	O	Clock output CLK5. 1MHz to 156.25MHz, in 1kHz steps, from Synthesizer G_5, or Synthesizer G_{T4} (T4); 2kHz, 8kHz or proprietary composite signal from Synthesizer F. LVCMOS.
CLK6	93	O	Clock output CLK6. 1MHz to 156.25MHz, in 1kHz steps, from Synthesizer G_6 or Synthesizer G_{T4} (T4); 2kHz, 8kHz, or proprietary composite signal from Synthesizer F. LVCMOS.
CLK7	94	O	Clock output CLK7. 1MHz to 156.25MHz, in 1kHz steps, from Synthesizer G_7 or Synthesizer G_{T4} (T4); 2kHz, 8kHz, or proprietary composite signal from Synthesizer F. LVCMOS.
CLK8	95	O	Clock output CLK8. 1MHz to 156.25MHz, in 1kHz steps, from Synthesizer G_8 or Synthesizer G_{T4} (T4); 2kHz, 8kHz, or proprietary composite signal from Synthesizer F. LVCMOS.
CLK8K	30	O	8kHz frame pulse signal, 50% duty cycle or programmable pulse width (T0)
CLK2K	31	O	2kHz frame pulse signal, 50% duty cycle or programmable pulse width (T0)
SRCSW	18	I	Hard-wired manual reference pre-selection
MPU_MODE0	60	I	Bus interface: Intel, Motorola, Multiplex, SPI
MPU_MODE1	59	I	
MPU_MODE2	58	I	
$\overline{CS}$	70	I	SPI bus chip select
$\overline{WR}$	71	I	Write access for Intel, Motorola and Multiplex bus interface
$\overline{RD}$	72	I	Read access for Intel and Multiplex bus interface
ALE/SCLK	73	I	ALE: Address latch enable for Multiplex bus interface SCLK: Clock edge selection for SPI
RDY	75	O	Ready/Data Acknowledge for Intel, Motorola and Multiplex bus interface

Table 1: Pin Description

Pin Name	Pin #	I/O	Description
A0/SDI	69	I	A0~A6: Address pins for bus interface Intel and Motorola SDI: SPI bus data input CLKE: Clock edge selection for SPI
A1/CLKE	68	I	
A2	67	I	
A3	66	I	
A4	65	I	
A5	64	I	
A6	63	I	
AD0/SDO	83	I/O	AD0~AD7: Bus interface Intel and Motorola data pins Multiplex data and address pins SDO: SPI bus data output
AD1	82	I/O	
AD2	81	I/O	
AD3	80	I/O	
AD4	79	I/O	
AD5	78	I/O	
AD6	77	I/O	
AD7	76	I/O	
NC	3, 4, 17, 22, 24, 25, 26, 27, 28, 29, 44, 96, 97, 98, 100		No connection. Pins are recommended to be tied to ground

Register Map

Table 2: Register Map

Addr	Reg Name	Bits	Type	Description
0x00	Chip_ID	15-0	R	Chip ID = 0x5420
0x01				
0x02	Chip_Rev	7-0	R	Chip revision number
0x03	Chip_Sub_Rev	7-0	R	Chip sub-revision number
0x04	T0_M/S_Sts	0	R	Indicates T0 master/slave state
0x05	T0_Slave_Phase_Adj	15-0	R/W	T0 slave phase adjust, 2's complement, step in 0.1ns
0x06				
0x07	Fill_Obs_Window	3-0	R/W	Activity monitor: Leaky bucket fill observation window
0x08	Leak_Obs_Window	3-0	R/W	Activity monitor: Leaky bucket leak observation window
0x09	Bucket_Size	5-0	R/W	Activity monitor: Leaky bucket size
0x0A	Assert_Threshold	5-0	R/W	Activity monitor: Leaky bucket alarm assert threshold
0x0B	De_Assert_Threshold	5-0	R/W	Activity monitor: Leaky bucket alarm de-assert threshold
0x0C	Freerun_Cali	10-0	R/W	Freerun calibration, 2's complement, -102.4 to +102.3ppm, step in 0.1ppm
0x0D				
0x0E	Disqualification_Range	9-0	R/W	Reference disqualification range, 0 ~102.3ppm. The value is also specified as pull-in range
0x0F				
0x10	Qualification_Range	9-0	R/W	Reference qualification range, 0 ~102.3ppm.
0x11				
0x12	Qualification_Soaking_Time	5-0	R/W	Reference qualification soaking time, 0 ~63s
0x13	Ref_Index_Selector	3-0	R/W	Select a reference input to access the register Ref_Info and Ref_Acceptable_Freq.
0x14	Ref_Info	15-0	R	Frequency offset and frequency info of the reference selected by register Ref_Index_Selector
0x15				
0x16	Ref_Activity	12-0	R	Reference activity for reference 1 to 12 and cross ref
0x17				
0x18	Ref_Qual	11-0	R	Reference 1 ~ 12 qualification
0x19				
0x1A	Interrupt_Event_Status	7-0	R/W	Interrupt events
0x1B	Interrupt_Event_Enable	7-0	R/W	Selects which of interrupt events will assert pin EVENT_INTR
0x1C	Interrupt_Config	1-0	R/W	Pin EVENT_INTR configuration and idle mode
0x1D	Hard-Wired_Switch_Pre_Selections	7-0	R/W	Pre-selected reference number 1 and reference number 2 for hard-wired manual switch mode
0x1E	SRCSW_Status	0	R	Indicates the status of pin SRCSW
0x1F [1]	T0/T4_Tag_Select	0	R/W	Selects registers between T0 and T4 for register 0x20 - 0x3F
0x20	Control_Mode	7-2	R/W	Holdover history usage, Revertive, Manual/Auto, OOP, Slave inherit, SRCSW
0x21	Loop_Bandwidth	7-0	R/W	Loop bandwidth selection
0x22	Auto_Elect_Ref	3-0	R	Indicates the reference elected by auto reference elector
0x23	Manual_Select_Ref	3-0	R/W	The reference specified by users for manual selection mode
0x24	Selected_Ref	3-0	R	Indicates the PLL current selected reference

Table 2: Register Map

Addr	Reg Name	Bits	Type	Description
0x25	Device_Holdover_History	31-0	R	Device Holdover History
0x26				
0x27				
0x28				
0x29	Long_Term_Accu_History	31-0	R	Long term Accumulated History
0x2A				
0x2B				
0x2C				
0x2D	Short_Term_Accu_History	31-0	R	Short term Accumulated History
0x2E				
0x2F				
0x30				
0x31	User_Specified_History	31-0	R/W	User programmed holdover history
0x32				
0x33				
0x34				
0x35	History_Ramp	7-0	R/W	Control long term history and short term history accumulation bandwidth and the locking stage's frequency ramp control
0x36	Ref_Priority_Table	47-0	R/W	REF1-12 selection priority
0x37				
0x38				
0x39				
0x3A				
0x3B				
0x3C	PLL_Status	7-0	R	PLL status: SYNC, LOS, LOL, OOP, SAP, FEE, DHT, HHA
0x3D	Holdover_Accu_Flush	0	W	Flush/reset the long-term history and the device holdover history
0x3E	PLL_Event_Out	7-0	R/W	PLL event out (Reserved)
0x3F	PLL_Event_In	7-0	R/W	PLL event in: Relock
0x40	EX_SYNC_Edge_Config	0	R/W	Select framing edge for EX_SYNC (falling or rising edge)
0x41	Slave_Frame_Align	3-0	R/W	Select cross ref source and frame edge for slave T0 timing generator
0x42	Master_Frame_Align	47-0	R/W	T0 timing generator selects the frame phase alignment and frame alignment working manner in master mode. Not for T4 timing generator.
0x43				
0x44				
0x45				
0x46				
0x47				
0x4A	Synth_Index_Select	3-0	R/W	Determine which synthesizer is selected for setting frequency value at register Synth_Freq_Value and adjusting phase skew at registers Synth_Skew_Adj
0x4B	Synth_Freq_Value	17-0	R/W	Selects synthesizer frequency value from 1MHz to 156.25MHz, in 1kHz steps, based on which synthesizer index is selected at the register Synth_Index_Select
0x4C				
0x4D				
0x4E	Synth_Skew_Adj	11-0	R/W	Adjust phase skew for the synthesizer with the index selected at register Synth_Index_Select
0x4F				

Table 2: Register Map

Addr	Reg Name	Bits	Type	Description
0x50	CLK1/2_Signal_Level	1-0	R/W	Select the signal level (LVDS or LVPECL) for clock outputs CLK1 and CLK2
0x51	CLK1_Sel	1-0	R/W	Select synthesizer or enable tri-state for CLK1
0x52	CLK2_Sel	1-0	R/W	Select synthesizer or enable tri-state for CLK2
0x53	CLK3_Sel	1-0	R/W	Select synthesizer or enable tri-state for CLK3
0x54	CLK4_Sel	1-0	R/W	Select synthesizer or enable tri-state for CLK4
0x55	CLK5_Sel	1-0	R/W	Select synthesizer or enable tri-state for CLK5
0x56	CLK6_Sel	1-0	R/W	Select synthesizer or enable tri-state for CLK6
0x57	CLK7_Sel	1-0	R/W	Select synthesizer or enable tri-state for CLK7
0x58	CLK8_Sel	1-0	R/W	Select synthesizer or enable tri-state for CLK8
0x59	Frame8K_Sel	6-0	R/W	8kHz frame pulse clock duty cycle selection, signal inversion
0x5A	Frame2K_Sel	6-0	R/W	2kHz frame pulse clock duty cycle selection, signal inversion
0x5B	Ref_Acceptable_Freq	14-0	R/W	Select integer N for manually acceptable frequency at Nx8kHz; Enable auto detection of reference input frequency
0x5C				
0x5D	Frame_Mux	11-0	R/W	Select one of frame signal (Frame8K, Frame2K, or composite signal) and forward it to CLK3~CLK8 selection individually
0x5E				
0x5F	Diff_REF_Polarity	1-0	R/W	Differential input REF(11~12)_P and REF(11~12)_N polarity reverse
0x70	Field_Upgrade_Status	2-0	R	Indicates the status of field upgrade process
0x71	Field_Upgrade_Data	7-0	R/W	Load 7600 bytes of firmware configuration data
0x72	Field_Upgrade_Count	12-0	R	Count byte numbers that have been loaded
0x73				
0x74	Field_Upgrade_Start	7-0	W	Write three values consecutively to start the field upgrade process
0x7F	MCLK_Freq_Reset	7-0	R/W	Select the frequency of the external oscillator

Note 1: Timing generator T0 and T4 share register 0x20 ~ 0x3F. Register 0x1F selects between T0 and T4 for the sharing registers 0x20 ~0x3F.

Master Clock Frequency

The STC5420 supports four different frequencies of master clock: 10MHz, 12.8MHz, 19.2MHz, and 20MHz. See Chip Master Clock for details. Initial default accepted frequency of MCLK is 12.8MHz.

Table 3: Master Clock Frequency

12.8MHz (Initial default frequency)
10MHz
19.2MHz
20MHz

Input and Output Frequencies

Input Frequencies

Auto-Detect Acceptable Input Frequencies

The STC5420 can automatically detect the frequency of the reference input when the user enable the auto-detect function at the register **Ref Index Selector** and **Ref Acceptable Freq** for REF1~REF12 individually. REF11 and REF12 are LVPECL/LVDS. The acceptable frequency for auto detection is shown in Table 4.

Table 4: Auto-Detect Acceptable Ref Input Frequencies

Reference Input	Frequency
REF1 ~ REF 12	8 kHz
	64 kHz
	19.44 MHz
	38.88 MHz
	77.76 MHz
	1.544 MHz
	2.048 MHz
	6.48 MHz
	8.192 MHz
	16.384 MHz
	25 MHz
	50 MHz
	125 MHz
REF7[2]	Proprietary Composite signal
EX_SYNC[3]	Proprietary Composite signal, 2kHz or 8kHz external frame sync inputs

Manually Acceptable Input Frequencies

STC5420 provides another option which allows the user to select the manually acceptable reference frequency for REF1~REF12 individually, at the integer multiple of 8kHz (Nx8kHz, N is integer from 1 to 32767). Hence the manually acceptable reference frequency range is 8kHz to 262.136MHz, in 8kHz steps. When a manually acceptable reference frequency is used, the user need to access the register **Ref Acceptable Freq** to set the integer N for associated reference input selected at the register **Ref Index Selector**.

Input Frequency = N x 8kHz, where N = 1~32767

Note 2:
In slave mode configuration, REF7 can also accept proprietary composite signal as input besides the high frequencies shown in Figure 3.

Note 3:
In both master and slave mode configuration, EX_SYNC may accept proprietary composite signal and 2kHz or 8kHz external frame reference inputs.

Clock Output Frequencies

Table 5: Available Clock Output Frequencies

CLK	CLK Level	Synthesizer	Clock Output Frequency Range
CLK1	LVPECL/LVDS	G_1	1MHz ~ 156.25MHz, in 1kHz steps
CLK2	LVPECL/LVDS	G_2	1MHz ~ 156.25MHz, in 1kHz steps
CLK8K	LVCMOS	F	Frame8K at 8kHz
CLK2K		F	Frame2K at 2kHz
CLK3	LVCMOS	G_3, F or G_{T4}	1MHz ~ 156.25MHz, in 1kHz steps; Frame8K/Frame2K at 8kHz/2kHz
CLK4	LVCMOS	G_4, F or G_{T4}	1MHz ~ 156.25MHz, in 1kHz steps; Frame8K/Frame2K at 8kHz/2kHz
CLK5	LVCMOS	G_5, F or G_{T4}	1MHz ~ 156.25MHz, in 1kHz steps; Frame8K/Frame2K at 8kHz/2kHz
CLK6	LVCMOS	G_6, F or G_{T4}	1MHz ~ 156.25MHz, in 1kHz steps; Frame8K/Frame2K at 8kHz/2kHz
CLK7	LVCMOS	G_7, F or G_{T4}	1MHz ~ 156.25MHz, in 1kHz steps; Frame8K/Frame2K at 8kHz/2kHz
CLK8	LVCMOS	G_8, F or G_{T4}	1MHz ~ 156.25MHz, in 1kHz steps; Frame8K/Frame2K at 8kHz/2kHz

Clock Output Jitter

Table 6: Clock Output Jitter

Clock Output	Frequency	RMS jitter[4] (Typical)	pk-pk jitter[4] (10^{-12}) (Typical)	
	(MHz)	(ps)	(ps)	(UI)
CLK1/CLK2 (LVPECL/LVDS)	156.25	13	210	0.03
	155.52	13	210	0.03
	125	13	210	0.03
	77.76	13	210	0.02
CLK3~CLK7 (LVCMOS)	77.76	19	330	0.03
	38.88	16.5	280	0.01
	19.44	15	230	0.005
	25	13	180	0.005
	2.048	11	180	0.0004
	1.544	11	160	0.0003

Note 4: Filter bandwidth is from 12kHz to Frequency/2

General Description

Application

The STC5420 is a single chip solution for the synchronous clock in SDH (SETS), SONET, and Synchronous Ethernet network elements. The device is fully compliant with ITU-T G.813 (option1 and option2), G.8262 EEC (option1 and option2), Telcordia GR1244, and GR253 (Stratum3/4E/4/SMC). Its highly integrated design implements all necessary reference selection, monitoring, filtering, synthesis, and control functions. An external oscillator (e.g., high precision OCXO or TCXO) completes a system level solution (see Functional Block Diagram, Figure 1). The STC5420 has four programmable frequency options of external oscillator. The STC5420 supports master/slave and multiple-master operations for redundant application.

Overview

The STC5420 accepts 12 reference inputs and generates 10 synchronized clock outputs, including 2 frame pulse clock outputs CLK8K and CLK2K at 8kHz and 2kHz. Two independent PLL-based timing generators, T0 and T4, provide the essential functions for Synchronous Equipment Timing Sources (SETS). T0 controls synthesizers G_1~G_8, and synthesizer F. T4 controls synthesizer G_{T4}. Clock outputs CLK1~CLK8 can be derived from synthesizer G_1~G_8, respectively. CLK3~CLK8 can also be derived from synthesizer F through T0 path or synthesizer G_{T4} through T4 path. Frame pulse clock outputs are derived from synthesizer F. The STC5420 incorporates a microprocessor interface, which can be configured for all common microprocessor interface types.

Chip Master Clock

The STC5420 operates with an external oscillator (e.g., OCXO or TCXO) as its master clock. The device supports four different frequencies of master clock: 10MHz, 12.8MHz, 19.2MHz, and 20MHz. Initial default accepted frequency is 12.8MHz.

Reference Inputs

The STC5420 accepts 12 reference inputs. REF11 and REF12 are LVPECL/LVDS, remaining 10 are LVCMOS. The 12 reference inputs are continuously activity and quality monitored. The reference inputs may be selected to accept either the auto-detect acceptable reference frequency which can be automatically detected by STC5420 or manually acceptable reference frequency. The activity monitoring is implemented with a programmable leaky bucket algorithm.

A reference is designated as “qualified” if it is active and its fractional frequency offset is within the programmed range for a programmed soaking time. An auto reference elector elects the most appropriate one from the reference inputs according to the revertivity status, and each reference’s priority and qualification. Revertivity determines whether a higher priority qualified reference should preempt a qualified current auto-elected reference. If none of the references input is qualified, holdover or freerun mode will be elected depending on the availability of the holdover history.

Reference selection may be automatic, manual, or hard-wired manual. In automatic reference selection mode, the most appropriate one elected from the auto reference elector will be the selected reference input. In manual reference selection mode, user may specify any of the reference inputs as the selected reference input for external timing or holdover/freerun for self-timing. In hard-wired manual mode, user can fast switch using control pin SRCSW between two preprogrammed reference inputs. The reference input elected from the auto reference elector will not affect the selected reference input in manual or hard-wired manual mode.

In manual reference selection mode, the timing generator T4 may accept T0’s synchronized output as its input.

Timing Generators and Operation Modes

The STC5420 includes two independent timing generates, T0 and T4, to provide the essential functions for SETS. Each timing generator can individually operate in ***Freerun***, ***Synchronized***, ***Pseudo-Holdover*** and ***Holdover*** mode. A timing generator is in either external-timing mode or self-timing mode. In external timing mode, PLL of the timing generator phase locks to the selected external reference input. In self-timing mode, the PLL simply tunes the clock

synthesizers to a given fractional frequency offset. Synchronized mode is in external timing. PLL's loop bandwidth may be programmed individually to vary the timing generator's filtering function. Conversely, freerun, pseudo-holdover and holdover modes are all in self-timing. When selected reference input and previous holdover history are unavailable, such as in system's initialization stage, freerun mode may be entered or used. When selected reference input is unavailable but a long-term holdover history accumulated in previous synchronized mode is available, holdover mode may be entered or used. STC5420 may enter pseudo-holdover using short-term frequency history. In STC5420, the freerun clock is derived from the MCLK (external oscillator) and digitally calibrated to compensate the external oscillator's accuracy offset. STC5420 also allow users to program and manipulate the holdover history accumulators.

Phase Synchronization

In synchronized mode, the phase relationship between the selected reference input and the clock output may be phase arbitrary or frame phase align for T0 timing generator. For timing generator T4, the phase relationship is only phase arbitrary. Zero frame phase relationship is produced for T0 timing generator by programming as frame phase align mode. Switching to a new reference input may expect a longer pull-in process in this mode. On the other hand, programming as arbitrary mode, an arbitrary phase relationship incorporates phase rebuild on reference input switching to minimize the downstream clock's phase transient. In this scenario, the STC5420 can provide hit-less switching if both reference inputs are traced to the same clock source (e.g., PRC). The STC5420 may accept external frame reference to achieve frame alignment in frame phase align mode. The frame reference and the frame edge, and frame phase alignment mode may be configured independently for each individual reference input.

A maximum frequency ramp may be programmed to minimize the ramp of fractional frequency offset changing in the case that the new selected reference is not traced to the same source. This feature restrains the frequency transient which may cause the pull-out-of- lock of the downstream network elements.

Clock Outputs

The STC5420 outputs 10 synchronized clock outputs: 2 differential clock outputs (LVPECL or LVDS) CLK1 and CLK2, 6 LVCMOS clock outputs CLK3 to CLK8 (LVCMOS), one CLK8K and one CLK2K frame pulse clock outputs (LVCMOS). CLK1~CLK8 can be derived from synthesizer G_1~G_8 through T0 path, respectively, in which CLK3~CLK8 can also be derived from synthesizer F through T0 path or synthesizer G_{T4} through T4 path. See Figure 1 for functional details. Frequency of clock outputs CLK1~CLK8 is programmable by programing frequency of the associated synthesizer from 1MHz up to 156.25MHz, in 1kHz steps. Each of the synthesizers has different default frequency value. The STC5420 allows the user to program the phase skew of each clock synthesizer, up and down 50ns in roughly 0.024ns step to adjust the phase of clock outputs.

Frame pulse clock synthesizer F generates frame pulse clock Frame8K/Frame2K at frequency of 8kHz/2kHz and a proprietary composite signal which carries 8kHz clock, 2kHz frame, and the selected reference information. The duty-cycle of Frame8K and Frame2K is programmable. Clock outputs CLK8K and CLK2K are directly driven from Fram8K and Frame2K.

Redundant Designs

Timing generator T0 supports ***master/slave*** and ***multiple-master*** operation for redundant applications to allow system protection against the failure of the single unit.

In master/slave configuration, the slave unit phase-locks and frame aligns (8kHz or 2kHz) to the cross-reference from the master unit, using highest available loop bandwidth and ignores any frequency ramp protection. The phase of slave's clock outputs may be adjusted up and down 3.2us, in 0.1ns step, to compensate for the propagation and re-transmission delay of the cross-couple path. This will then minimize the phase hits to the downstream devices resulting from master/slave switches.

In multiple-master configuration, all units work as masters and lock to the same reference input in parallel. With the help of frame phase align mode and the extra frame edge, clock outputs of all the units may keep in frame phase alignment. No phase compensa-

tion as in master/slave configuration. In order to meet same synchronization requirement, each unit should use same parameter setup including loop bandwidth. Multiple-master configuration demands a high quality external oscillator to obtain a precise frame phase alignment.

Control Interfaces

The STC5420's controls interfaces are composed of hardwire control pins and the bus interface. They provide application access to the STC5420ís internal control and status registers. This bus interface may be configured among four type of micro-controller interfaces, three of them are in parallel (Intel, Motorola, Multiplexed) and one in serial (SPI). The selection of the bus interface is pin-controlled.

Field Upgradability

The STC5420 supports Field Upgradability which allows the user to load size of 7600 byte firmware configuration data (provided as per request) via bus interface. It provides the user a flexible field solution for different applications.

Advantage and Performance

The kernel of each timing generator is a DSP-based PLL. In STC5420, all internal modules are either digital or numerical, including the phase detectors, filters, and clock synthesizers. The revolutionary pure-digital design makes the timing generator become an accurate and reliable deterministic system. This modern technology removes any external component except the external oscillator. It provides excellent performance and reliability to STC5420. A well-chosen oscillator will make STC5420 meet all the synchronization requirements. Short-term stability associated with the desired loop bandwidth is a more important factor than aging projection and thermal response when select an appropriate oscillator.

Detailed Description

The STC5420 is a single chip solution for the synchronous clock in SDH (SETS), SONET, and Synchronous Ethernet network elements. The revolutionary pure-digital internal modules, DSP-based PLL and clock synthesizer are used in the device so that the overall characteristics are more stable compared to traditional method.

Chip Master Clock

The device operates with an external oscillator (e.g., OCXO or TCXO) as its master clock, connected to the MCLK input, pin 10. Generally, user should select an oscillator has great stability and low phase noise as the master clock (MCLK).

The STC5420 supports four different accepted frequencies of master clock: 10MHz, 12.8MHz, 19.2MHz, and 20MHz. Initial default accepted frequency of MCLK for STC5420 is 12.8MHz. When 10MHz, 19.2MHz, or 20MHz is selected as the frequency of MCLK, the user must write register **MCLK Freq Reset** three times consecutively, with no intervening read/writes from/to other register. An internal soft-reset will occur after three writes completed. The accepted frequency of MCLK input returns to 12.8MHz following any regular reset. See register **MCLK Freq Reset** for details.

In the meantime, the STC5420 allows user to read three values at the register **MCLK Freq Reset**: FRQID, COUNT, and ID Written Value.

FRQID
Indicates the ID of the frequency of MCLK that the STC5420 currently accept.

COUNT
Indicates how many times the register **MCLK Freq Reset** has been written to.

ID Written Value
Indicates the ID of associated value that is being written to the register **MCLK Freq Reset**.

See the register **MCLK Freq Reset** for more details.

Freerun Clock

The STC5420 has an internal freerun clock synthesized from the MCLK. The frequency offset of the internal freerun clock can be calibrated by writing to the register **Freerun Cali**. It has the stability of the external TCXO/OCXO. The calibration offset may be programmed in 0.1ppm steps from -102.4 to +102.3ppm, in 2's complement. This feature allow the user can digitally calibrate the freerun clock without physically adjusting the local oscillator.

Operation Mode

The STC5420 includes two timing generators, T0 and T4 timing generators. Each timing generator has its own PLL and can be individually operate in either external-timing or self-timing mode. In external timing mode, PLL of a timing generator phase-locks to a reference input. In self-timing mode, PLL simply operates with the external oscillator (MCLK). The STC5420 supports four operation modes: *freerun* (self-timing), *synchronized* (external-timing), *pseudo-holdover* (self-timing) and *holdover* (self-timing).

Freerun Mode
Freerun mode is typically used during system's initialization stage when none of reference inputs is available and the clock synchronization has not been achieved. The clock output generated from the STC5420 in freerun mode is based on the internal freerun clock which is synthesized from MCLK. Frequency of the internal freerun clock can be calibrated by writing to the register **Freerun Cali**.

Synchronized Mode
In synchronized mode, the built-in PLL of the timing generator locks to the selected reference input. Each timing generator's loop bandwidth is independently programmable from 0.1Hz to 100Hz by writing to the register **Loop Bandwidth**. The noise transfer function of the PLL is determined accordingly by the loop bandwidth and has maximum gain under 0.2dB. In synchronized mode, the phase relationship between the reference input and the clock output can be configured as arbitrary or aligned for timing generator T0 at register **Master Frame Align**. Timing generator T4 operates only in phase arbitrary.

Pseudo-Holdover Mode
In pseudo-holdover mode, the clock is synthesized from the MCLK and an accumulated short-term his-

tory. This history is accumulated by a built in programmable short-term history accumulator consecutively, which presents the latest updated fractional frequency offset of the synchronous clock output of each timing generator. The user can read the short-term history from register **Short Term Accu History**.

Holdover Mode

Holdover mode is typically used when none of reference inputs is available and the holdover history has been built. In holdover mode, the frequency offset of the clock output is maintained closely to previous value generated when the selected reference input was valid. User can select either device holdover history or user specified holdover history at the register **Con- trol Mode** in holdover mode.

PLL Event In

The STC5420 provides direct communication with the PLL's timing generator by writing to the register **PLL Event In**. Following events can be triggered:

- **Relock**. PLL starts a relock process if this event is triggered. In frame phase align mode, PLL relocks to the reference input and the frame edge is re-selected as well. In phase arbitrary mode, PLL relocks to the reference input and restart the phase rebuild process.

Frequency and Phase Transients

Severe frequency and phase transients of the clock output will cause lost of lock or buffer overflow/underflow on downstream circuit. By providing programmable maximum slew rate and phase rebuild function, both frequency and phase transient of the STC5420's clock output is controlled to minimize the impact on downstream circuits.

Frequency Transients

The STC5420 smoothly control the frequency transient on the clock output. During reference input switching or operation mode switching (etc., switch to freerun or holdover mode), if the clock output prior to switching has different frequency offset than the desired clock output, it smoothly approaches to desired frequency offset with a maximum acceleration/decel- eration rate by writing to the register History Ramp. The maximum slew rate can be programmed as 1.0, 1.5, 2.0 ppm/second. With a limited acceleration/ deceleration, the pull-in process may last longer. However, it will minimize the frequency transient impact to the downstream clock and ensure meeting components frequency impact tolerance.

Phase Transients

The STC5420 minimize the variation of the phase transient on the clock output when a phase hit occurs on the selected reference input. The overshoot in the clock output's phase transient response will be a small amount under 2%.

During reference input switching or recovering from LOS/LOL condition, the phase transient is also occurred on the clock output. The STC5420 can minimize it with a phase rebuild function. In synchronized mode, the phase relationship between the reference input and the clock output can be programmed to phase arbitrary or frame phase align at the register **Master Frame Align**. If phase arbitrary is selected, a phase rebuild function is performed before locking to the new/recovered reference input. Hit-less switching is achieved with this function and the phase hit to downstream circuits is eliminated. If frame phase align is selected, the clock output is in frame phase alignment with the reference input. Only T0 timing generator supports frame phase alignment.

History of Fractional Frequency Offset

The STC5420 monitors and tracks the fractional frequency offset between the clock output and MCLK. The history data of the frequency offset is used by clock synthesizers to generate desire outputs while the timing generator is pending for reference input availability. Two weighted 3rd order low-pass filter are used internally as two history accumulators: the short term history accumulator and the long term history accumulator. A mature long term history is stored and further updated as device holdover history. It is used when the STC5420 operates in holdover mode. In addition, the STC5420 allows user to program an user specified history as needed of the application.

Short-Term History

Short-term history is an average frequency offset between the clock output and MCLK which is filtered internally using a weighted 3rd order low-pass filter with the small time constant. The -3dB filter response point can be programmed from 0.16Hz to 1.3Hz by writing to the register **History Ramp register**. Short-

term history can be read from the register **Short_Term_Accu_History**. Typically, short-term history is used by clock synthesizer in two conditions: First, it is used in between the transition of two different operation modes; second, it is used if LOS occurs when the STC5420 operates in synchronized mode with manually reference selection.In addition, short-term history is provided to perform failure diagnostics and evaluations.

Long-Term History

Long-term history is an average frequency offset between the clock output and MCLK which is filtered internally using a weighted 3rd order low-pass filter with the long time constant. The -3 dB filter response point can be programmed from 0.15mHz to 1.3Hz by writing to the register **History Ramp**. The history value can be read from the register **Long Term Accu History**.

Device Holdover History

Device holdover history is the history data used when the STC5420 runs in holdover mode. It is acquired from the long term history previously described. In synchronized mode, when timing generators PLL has locked to the selected reference input for over 15 minutes, the long term history is stored and further updated as the device holdover history. If LOS or LOL occurs, the device holdover history will stay at the latest updated value until re-enter the synchronized mode and the PLL locks to the replaced selected reference input for another 15 minutes. Set Bit HO_Usage bit of the register **Control Mode** to select using device holdover history. Its value can be read from the register **Device Holdover History**.

User-Specified History

The STC5420 allows user to provide the history data created from their own sophisticated history accumulation algorithms by writing to the register **User Specified History**. Set bit HO_Usage of the register **Control Mode** to select using user specified holdover history. Its value can be read from the register **User Specified History**.

Phase-Locked Loop Status Details

The register **PLL Status** contains the detailed status of the PLLs, including the signal activity of the selected reference, the synchronization status, and the availability of the holdover histories.

SYNC bit

In external-timing mode, this bit indicates the achievement of synchronization. This bit will not be asserted in self-timing mode.

LOS bit

In external-timing mode, this bit indicates the loss of signal on the selected reference. This bit will not be asserted in self-timing mode.

LOL bit

In external-timing mode, the bit will be set if the PLL fails to achieve or maintain lock to the selected reference. This bit will not be asserted in self-timing mode. It is also not complementary to the SYNC bit. Both bits will not be asserted when the PLL is in the pull-in process. The pull-in process usually occur when switch to a new selected reference or recover from the LOS/LOL.

OOP bit

This bit indicates that the selected reference is out of the pull-in range. This is meaningful only if in external-timing mode. This bit will not be asserted in self-timing mode. The frequency offset is relative to the digitally calibrated freerun clock.

SAP bit

This bit when set indicates that the PLL's output clocks have stopped following the selected reference because the frequency offset of the selected reference is out of pull-in range (OOP). User can write to the **Control Mode** register to program whether the PLL shall follow the selected reference outside of the specified pull-in range or just stay within the pull-in range boundary.

FEE bit

This bit indicates whether an error occurs in the frame edge detection process in slave mode or master phase align mode. For timing generator T0 only.

DHT bit

This bit indicates whether the device holdover history is tracking on the current selected reference (updating by the long-term history).

HHA bit

This bit indicates the availability of the holdover history, which may be either the user provided history or the device holdover history.

Reference Inputs Details

The STC5420 accepts 12 external reference inputs. The reference inputs may be selected to accept either the auto-detect acceptable reference frequency which can be automatically detected by STC5420 or manually acceptable reference frequency. Reference inputs REF11 and REF12 are LVPECL/LVDS and the remaining ten are LVCMOS. Signal polarity of REF11 and REF12 is reversible at the register **Diff Ref Polarity**. All 12 reference inputs are monitored continuously for frequency, activity and quality. Each timing generator may select any of the reference inputs when the device is in external timing mode. T4 may accept T0's output as its input via internal feedback path.

Acceptable Frequency and Frequency Offset Detection

The STC5420 can automatically detect the frequency of the reference input when the user enable the auto-detection function at the register **Ref Index Selector** and **Ref Acceptable Freq**. The acceptable auto-detect frequencies are: 8kHz, 64kHz, 1.544MHz, 2.048MHz, 19.44MHz, 38.88MHz, 77.76MHz, 6.48MHz, 8.192MHz, 16.384MHz, 25MHz, 50MHz or 125MHz. These frequencies can be automatic detected continuously in the detector. Any carrier frequency change will be detected within 1ms. Each input is also monitored for frequency offset between input and the internal freerun clock. The frequency offset is a key factor to determine qualification of the reference inputs. See register **Ref Index Selector** and **Ref Info**.

STC5420 provides another option which allows the user to select the manually acceptable reference frequency for all the reference inputs, at the integer multiple of 8kHz (Nx8kHz, N is integer from 1 to 32767). Hence the manually acceptable reference frequency range is integer multiple of 8kHz from 8kHz to 262.136MHz. When a manually acceptable reference frequency is used, the user need to access the register **Ref Acceptable Freq** to set the integer N for the reference input which is selected at the register **Ref Index Selector**. Each input is monitored for frequency offset between input and the internal freerun clock. The frequency offset is shown in the register **Ref Info** when associate reference index is selected at the register **Ref Index Selector**.

Activity Monitoring

Activity monitoring is also a continuous process which is used to identify if the reference input is in normal. It is accomplished with a leaky bucket accumulation algorithm, as shown in Figure 2. The "leaky bucket" accumulator has a fill observation window that may be set from 1 to 16ms, where any hit of signal abnormality (or multiple hits) during the window increments the bucket count by one. The leak observation window is 1 to 16 times the fill observation window. The leaky bucket accumulator decrements by one for each leak observation window that passes with no signal abnormality. Both windows operate in a consecutive, non-overlapping manner. The bucket accumulator has alarm assert and alarm de-assert thresholds that can each be programmed from 1 to 64.

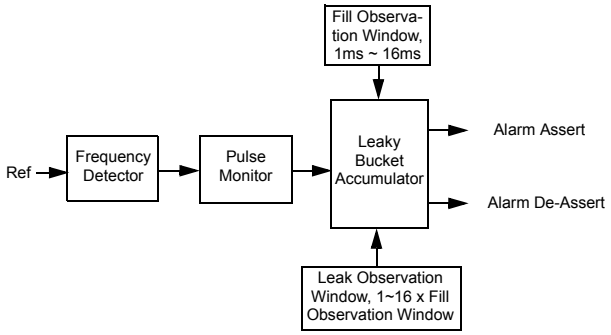


Figure 2: Activity Monitor

Applications can write to the following registers to configure the activity monitor: **Fill Obs Window**, **Leak Obs Window**, **Bucket Size**, **Assert Threshold**, and **De Assert Threshold**.

Setting the bucket size to 0 will bypass the leak bucket accumulator and assert or de-assert the activity alarm based on results of frequency detector and pulse monitor only. A non-zero bucket size must be greater than or equal to the alarm assert threshold value. The alarm assert threshold value must be greater than the alarm de-assert threshold value and less than or equal to the bucket size value. Attempted writes of invalid values will be ignored. Therefore, user must carefully plan an appropriate sequence of writes when re-configure the activity monitor. See register **Bucket Size**, **Assert Threshold** and **De Assert Threshold** for details.

Alarms appear in the **Refs Activity** register. A "1" indicates activity, and a "0" indicates an alarm, no activity. Note that if a reference is detected as a different frequency, the leaky bucket accumulator is set to the bucket size value and the reference will become inactive immediately.

Input Qualification

A selected reference is "qualified" if it passes the activity evaluation and its frequency offset is within the programmed qualification range for over a pre-programmed soaking time.

A reference qualification range may be programmed up to 102.3 ppm by writing to register **Qualification Range**, and a disqualification range set up to 102.3 ppm, by writing to register **Disqualification Range**. The qualification range must be set less than the disqualification range. Additionally, qualification soaking time may be programmed from 0 to 63 seconds by writing to register **Qualification Soaking Time**. The pull-in range is the same as the disqualification range.

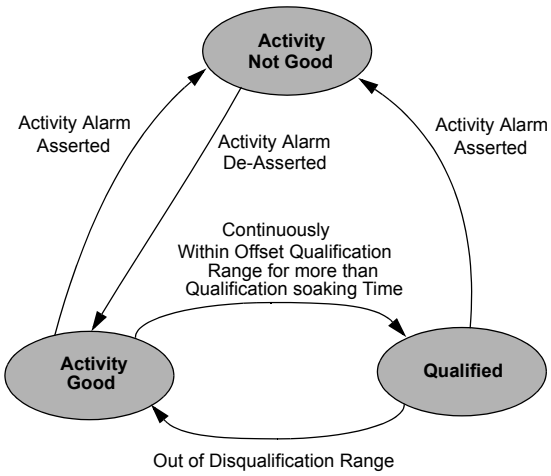


Figure 3: Reference Qualification Scheme

The frequency offset of each reference is relative to the internal freerun clock may be read by selecting the reference in the **Ref Index Selector** register and then reading the offset value from register **Ref Info**. The frequency offset of the internal freerun clock can be calibrated by writing to the register **Freerun Cali**.

Figure 3 shows the reference qualification scheme. A reference is qualified if it has no activity alarm and is continuous within the qualification range for more than the qualification soaking time. An activity alarm or frequency offset beyond the disqualification range will disqualify the reference. It may then be re-qualified if the activity alarm is off and the reference is within the qualification range for more than the qualification time.

The reference qualification status of each reference may be read from register **Ref Qual**.

Automatic Reference Election Mechanism

The STC5420 has an auto reference elector always elect the best candidate from the reference inputs according to the revertivity status, each reference's priority and qualification. T0 and T4 have independent priority tables for automatic reference selection. Regardless what the current reference selection mode is (automatic, manual, or hard-wired manual), the auto reference elector always work in this mechanism. The detail description of the reference selection mode is in following sections.

The reference priority is indicated in the reference priority table which is shown in register **Ref Priority Table** individually for each timing generator. Each reference has one entry in the table, which may be set to value from 0 to 15. '0' revokes the reference from the election, while 1 to 15 set the priority, where '1' has the highest, and '15' has the lowest priority. The highest priority pre-qualified reference then is a candidate selected by the automatic reference elector. If multiple references share the same priority, the one that has been qualified for the longest time will be recommended to be the candidate. If the current highest priority reference input fails, the next-highest priority reference is selected as the candidate.

In order to avoid disturbance of the clock output, the candidate reference selected by automatic reference elector should be handled in two different mode. Revertive mode and non-revertive mode. The mode is determined by either enabling or disabling the "revertive" bit of the **Control Mode** to "1" for revertive or to "0" for non-revertive operation.

In revertive mode, the automatic reference elector will pre-empted the current candidate reference if the new recommended candidate reference has higher priority.

In non-revertive mode, the current candidate refer-

ence will not be pre-empted by any new candidate until it is disqualified.

If there is no candidate reference available, freerun or holdover will be recommended by the automatic reference elector depending on the holdover history availability.

Figure 4 shows the operation states for automatic reference elector.

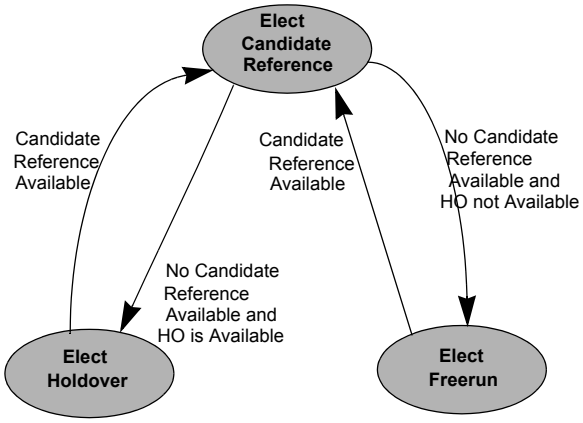


Figure 4: Automatic Reference Elector States

Automatic Reference Selection

The T0 and T4 timing generators may be individually operated automatic reference input selection mode. The mode is selected via the **Control Mode** registers.

In automatic reference selection mode, the selected reference is the same reference elected by the automatic reference elector. The automatically selected reference for each PLL may be read from the **Auto Elect Ref** registers.

Manual Reference Selection Mode

In manual reference selection mode, the user may select the reference manually. This mode is selected via the **Control Mode** registers. The reference is selected by writing to the **Manual Select Ref** registers. The user may also has the device enter freerun or holdover manually by writing to the **Manual Select Ref** registers. Besides, T4 may select T0's output as the selected reference.

Hard-wired Manual Reference Selection

Besides the manual reference selection mode, the STC5420 provides a special mode to switch between two pre-selected reference directly from a dedicated pin SRCSW. The two pre-selected references are configured at the register **Hard Wired Switch Pre Selection**. It can make the device enter the freerun or holdover by writing to the register **Hard Wired Switch Pre Selection**. In this mode, the pin SRCSW operates as a simple switch by setting high or low. Hard-wired Manual Reference Selection is for T0 only.

Clock Outputs Details

The STC5420 generates 2 synchronized differential (LVPECL or LVDS) clock outputs: CLK1 and CLK2; 6 LVCMOS clock outputs: CLK3~CLK8; frame pulse clock outputs CLK8K and CLK2K. Figure 5, Figure 6, and Figure 7 respectively shows the clock output section for CLK1/CLK2, CLK8K/CLK2K, and CLK3~CLK8. Each output has individual clock output section consist of a synthesizer and a clock generator. Clock generator of CLK1 or CLK2 has a LVPECL/LVDS driver to produce differential output. Each generator of CLK3~CLK8 includes two muxes and a LVCMOS signal driver. Generator of frame output CLK8K and CLK2K consist of a LVCMOS driver.

Clock Synthesizers

The STC5420 has 10 clock synthesizers, which of 9 is disciplined by the timing generator T0: synthesizer G1~G8 and one frame pulse clock synthesizer F; T4 disciplines a clock synthesizer G_{T4}. Clock synthesizers G_1~G_8 produce frequencies from 1MHz to 156.25MHz, in 1kHz steps. Phase skew of these synthesizers are all programmable individually up and down 50ns at the register **Synth Index Select** and **Synth Skew Adj**. CLK1 and CLK2 are derived from synthesizer G_1 and G_2. CLK3 ~ CLK8 can be derived from synthesizer G_3~G_8, also can be derived from synthesizer F or from synthesizer G_{T4} respectively. Synthesizer F produces frame pulse clock Frame8K, Frame2K, and a proprietary composite signal. Synthesizer F has two independent duty cycle controller for Frame8K and Frame2K which can program pulse width at the register **Frame8K Sel** and **Frame2K Sel**. Proprietary composite signal is a 3.3V LVCMOS data signal carries 8kHz clock, 2kHz frame, and the selected reference information.

Clock Generators

Clock generator of CLK1 or CLK2 consist of a LVPECL/LVDS signal driver. The signal level of clock outputs CLK1 and CLK2 can be programmed to either LVPECL or LVDS at the register **CLK1/2 Signal Level**. Clock generators of CLK3~CLK8 consist of a Frame Mux, CLK Sel Mux and a LVCMOS driver. CLK Sel Mux determines which synthesizer is selected for generator to output clock. When synthesizer F is selected, Frame Mux selects one of frame clocks (Frame8K, Frame2K, and proprietary composite signal) derived from synthesizer F and forward it to CLK Sel Mux for frame signal selection of CLK3~CLK8 individually. Frame Mux is set at the register **Frame Mux** and the CLK(3~8) Sel Mux is set at the registers **CLK(3~8) Sel** for CLK3 ~ CLK8 individually. Signal level of CLK3~CLK8 is driven from LVCMOS driver in clock generator.

The clock generator of CLK8K and CLK2K contains a LVCMOS driver. Clock outputs CLK8K and CLK2K output Frame8K and Frame2K clock pulse clock. The duty cycle is programmable at the register **Frame8K Sel** and **Frame2K Sel**.

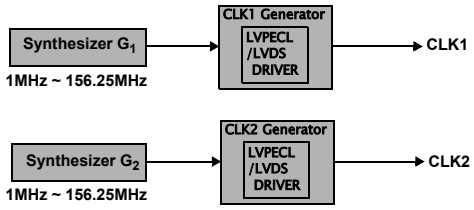


Figure 5:Output Clocks CLK1 and CLK2

Clock Output Phase Alignment

Any of clock outputs (except those derived from synthesizer G_{T4}) which has frequency at the integer multiple of 8kHz is in phase alignment with the frame pulse output CLK8K if none of synthesizer skew is programmed.

Synthesizer Skew Programming

The STC5420 allows user to program the phase skew of each clock synthesizer, up and down 50ns in roughly 0.024ns steps. Since each of clock outputs is dedicate derived from its synthesizer respectively, adjust phase skew of the synthesizer will provide the associated clock output a phase skew adjustment. Phase skew of the 10 synthesizers may be programmed at the register **Synth Index Select** and **Synth Skew Adj**.

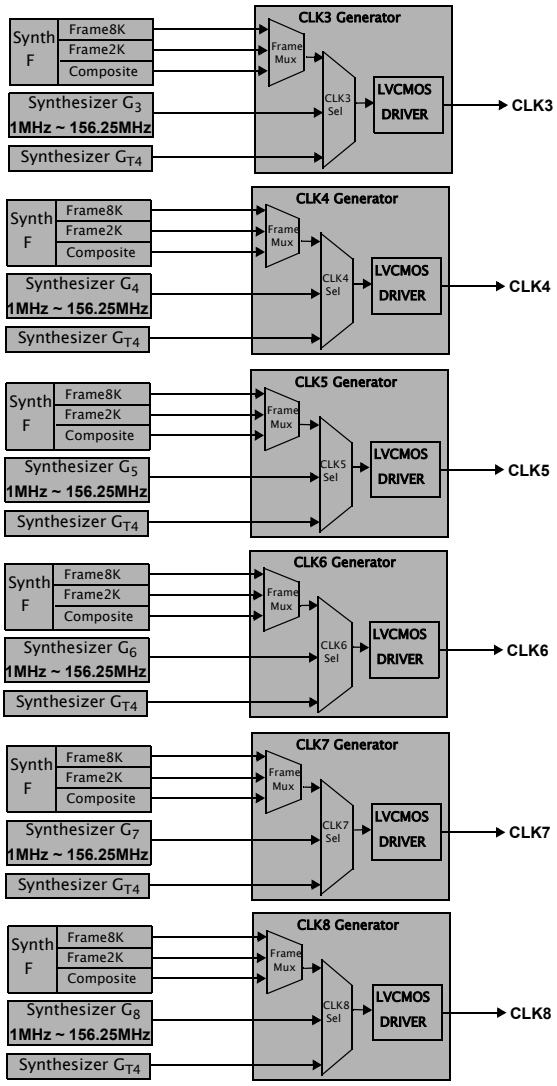


Figure 6:Output Clocks CLK3~CLK8

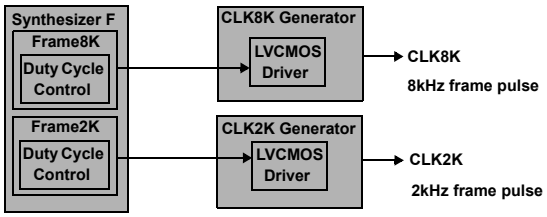


Figure 7:Output Clocks CLK8K and CLK2K

Clock Outputs

CLK1 or CLK2 is selected when associated synthesizer G_1 or G_2 is selected at the register **CLK1 Sel** or **CLK2 Sel**. Output frequencies or phase skew of CLK1 and CLK2 are programmable when frequency or skew of the associated synthesizer is programmed

at the register **Synth Index Select**, **Synth Freq Value**, and **Synth Skew Adj**. Output frequency is programmable from 1MHz to 156.25MHz, in 1kHz steps.

CLK3~CLK8 is selected when associated synthesizer G_3~G_8, or G_{T4} is selected at the register **CLK(3~8) Sel**. Output frequencies or phase skew of CLK3~CLK8 are programmable when frequency or skew of the associated synthesizer is programmed at the register **Synth Index Select**, **Synth Freq Value**, and **Synth Skew Adj**. Output frequency of CLK3~CLK8 is programmable from 1MHz to 156.25MHz, in 1kHz steps, via either synthesizer G_3~G_8 or G_{T4} individually. CLK3~CLK8 can also output frame pulse clocks when synthesizer F is selected at the register **CLK(3~8) Sel**. One of frame pulse clock of Frame8K, Frame2K, or proprietary composite signal is selected at the register **Frame Mux** for CLK3~CLK8 individually. Phase skew of frame pulse clocks is programmable simultaneously at the register **Synth Index Select** and **Synth Skew Adj**.

Redundant Application

Timing generator T0 supports master/slave and multiple-master operation for redundant applications to allow system protection against single part failure.

External Frame Reference Input

For redundant design, either in master/slave mode or multiple-master mode, all the timing devices should keep in frame phase alignment. In order to achieve the alignment, the frame edge of reference input is required. If the reference input is not proprietary composite signal or 8kHz input signal which contains its own frame information, an external frame reference input (at pin EX_SYNC) is used and some configuration enhancements are required. See register **Slave Frame Align** for slave mode configuration (when pin MC/$\overline{SL}$ = 0). See register **Master Frame Align** for master mode configuration (when pin MC/$\overline{SL}$ = 1).

Master Slave Configuration

Pairs of STC5420 devices may be operated in a master/slave configuration. Pin MC/$\overline{SL}$ determines each T0 timing generator of the two devices to work in master mode or slave mode. In master/slave configuration, slave device synchronizes and frame phase aligns with the master device and reverts to lock to the same external reference that the master device was locked to, using 100Hz loop bandwidth and ignores the loop bandwidth programmed at register **Loop Bandwidth**. In order to achieve master/slave frame phase alignment, two signals (one cross reference clock and one frame reference clock) or one signal (contains both cross reference and frame reference clock) is interconnected between the master and slave. The combination of cross reference and frame reference clock has four options:

1. High frequency output of master device feeds into REF7 of slave device as cross reference; Frame pulse 8kHz or 2kHz output of master device feeds into EX_SYNC of slave device as frame reference.
2. Frame pulse 8kHz output of master device feeds into EX_SYNC of slave device as cross reference and frame reference.
3. Proprietary composite signal of master device feeds into REF7 of slave device as cross reference and frame reference.
4. Proprietary composite signal of master device feeds into EX_SYNC as cross reference clock and frame reference.

To achieve 2kHz frame alignment, option 1, 3, or 4 should be selected. 8kHz on EX_SYNC pin cannot produce 2kHz frame alignment. See register **Slave Frame Align** for cross reference clock and frame reference clock selection details. If an error occurs when sampled on the selected frame edge of the cross reference, bit FEE of register **PLL Status** will be asserted. Master's frame pulse output CLK8K replace the selected frame reference input as the temporary frame reference. This error does not send alarm of synchronization faliure or loss of lock. User can invoke a relock event to PLL by programming the register **PLL Event In**. The frame edge is re-selected as well.

User can select either falling edge or rising edge for frame reference input EX_SYNC when the frame reference input on pin EX_SYNC is not composite signal. See the register **EX SYNC Edge Config**.

The proprietary composite signal contains not only cross reference clock and the frame reference clock of the master device but the information of the selected reference of the master device. Having this information, the slave unit is able to identify the selected reference of the master device. Therefore, in automatic reference selection mode, when the slave device takes it over to be the new master device, it can select the reference clock which previous master device was locked to by setting bit Slave Inherit Mode

of the register **Control Mode**. However, if the new master device operates in revertivity mode or has different qualification results than previous master device, it will select any preferred reference input.

In master/slave mode, for the latency delay on the cross-couple path, it may be compensated up and down 3.2μs, in 0.1ns step. This will then minimize the phase hits to the downstream devices resulting from master/slave switches.

Multiple Master Configuration

In multiple-master configuration, every unit works as master and locks to the same reference input. Each unit has consistent loop bandwidth settings. To achieve frame phase alignment for all the masters' outputs, each device has to choose same frame edge on the selected reference input clock. The system may provides every master a common extra frame reference or simply choose a 8kHz reference input.

Frame reference clock and frame edge on each reference input is configured at register **Master Frame Align**. If an error occurs when sampled on the selected frame edge of the selected reference, bit FEE of register **PLL Status** will be asserted and frame pulse output CLK8K replaces the selected frame reference input as the temporary frame reference. This error does not send alarm of synchronization faliure or loss of lock. User can invoke a re-lock event to PLL by programming the register **PLL Event In**. The frame edge is re-selected as well.

Multiple master configuration works only in frame phase align mode. By writing to the Master Frame Align register, user can set T0 timing generator to frame phase align mode with the frame edge selection.

To meet the same synchronization and frame alignment requirements, each unit should keep the same parameter setup, especially loop bandwidth. Multiple-master mode demands a high quality external oscillator to obtain a precise frame phase alignment.

Event Interrupts

The STC5420 events shown following below are interrupt events might occurred.

- Qualification status of the reference inputs change
- Activity status of the cross reference inputs change
- Selected reference of timing generator T0 changes in automatic reference selection
- Selected reference of timing generator T4 changes in automatic reference selection
- PLL status of timing generator T0 changes
- PLL status of timing generator T4 changes
- Out-Event of timing generator T0 asserts
- Out-Event of timing generator T4 asserts

The interrupt events can be read from **Interrupt Status** register. Each bit indicates one events. The associate bit of the **Interrupt Status** will not be changed automatically when the event is cleared. Therefore, the user need write '1' to the associate bit to erase the event.

The STC5420 has a pin EVENT_ INTR (pin 8) for indicating the event interrupt occurrence. The pin may be wired to user's micro-controller. User can program the **Interrupt Mask** register to decide which of interrupt events will send an alarm to the micro-controller by asserting the EVENT_INTR pin. User can program at the **Interrupt Configuration** register to specify the logic level (active high or low) of the pin EVENT_INTR when it's trigged by the interrupt event. User may also program the **Interrupt Configuration** register to define pin states as tri-state or logic inactive when no interrupt event occurs.

Field Upgradability

The STC5420 supports field upgradability which allows the user to load size of 7600 byte firmware configuration data (provided as per request) via bus interface. Field upgrade can only be performed at least 3ms after reset.

1. User may read Bit READY of the register **Field Upgrade Status** to check if field upgrade is ready to start.
2. To begin the field upgrade, write to register Field Upgrade Start three times consecutively, with no intervening read/writes from/to other registers, see the register **Field Upgrade Start** for details.
3. Once the field upgrade process begins, the STC5420 is hold for data loading. Write 7600 bytes firmware configuration data to the register **Field Upgrade Data** one byte at a time to complete data loading. User can read the same register for the written byte. But regardless of how many times the user read, only the last written byte will be read from the register.
4. Read the register **Field Upgrade Count** for how many bytes of configuration data has been loaded. Bit Load_Compelet of the register **Field Upgrade Status**

will indicate whether the 7600 bytes loading is complete and meanwhile bit CHECKSUM will indicate the loading is failed or succeed. See register description of **Field Upgrade Status** for details.

Processor Interface Descriptions

The STC5420 supports four common microprocessor control interfaces: SPI, Motorola, Intel, and Multiplex. The control interface mode is selected with the MPU_MODE(0/1/2):

MPU_MODE2 (Pin 58)	MPU_MODE1 (Pin 59)	MPU_MODE0 (Pin 60)	Bus Mode
0	0	1	Reserved
0	1	0	Multiplex
0	1	1	Intel
1	0	0	Motorola
1	0	1	SPI

The following sections describe each bus mode's interface timing:

SPI Bus Mode

The SPI interface bus mode uses the $\overline{CS}$, SCLK,SDI, SDO pins, with timing as shown in Figure 8, Figure 9 and Figure 10. For read operation, serial data output can be read out from the STC5420 on either the rising or falling edge of the SCLK. The edge selection depends on pin CLKE logic level.

Serial Bus Timing

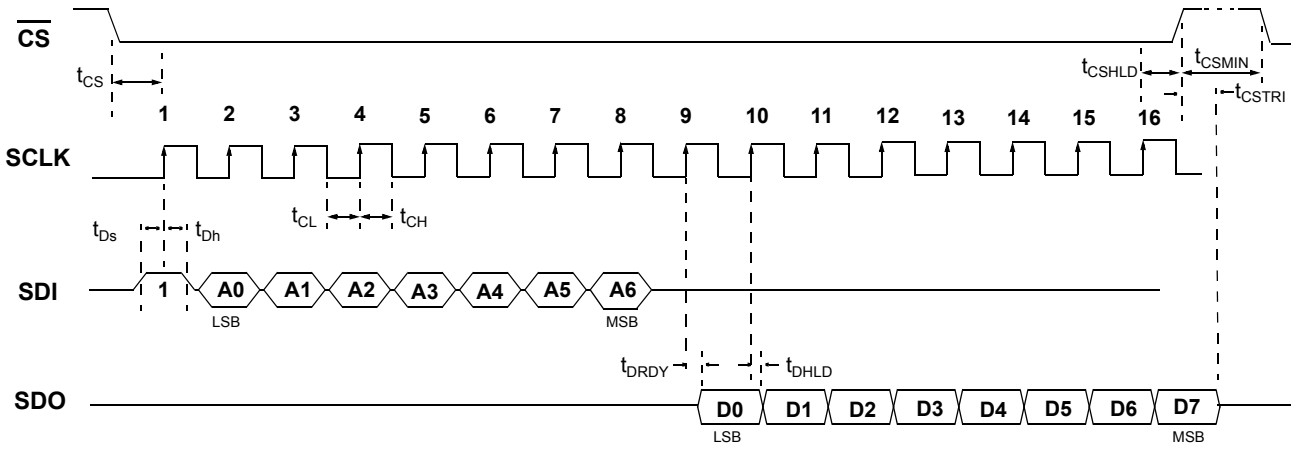


Figure 8:SPI Bus, Read access (Pin CLKE = Low)

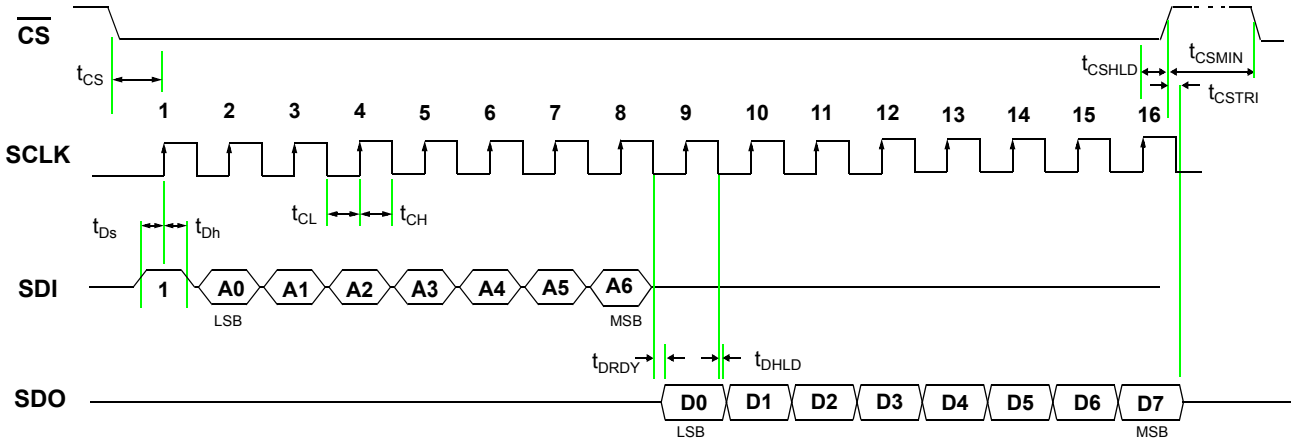


Figure 9: SPI Bus Timing, Read access (Pin CLKE = High)

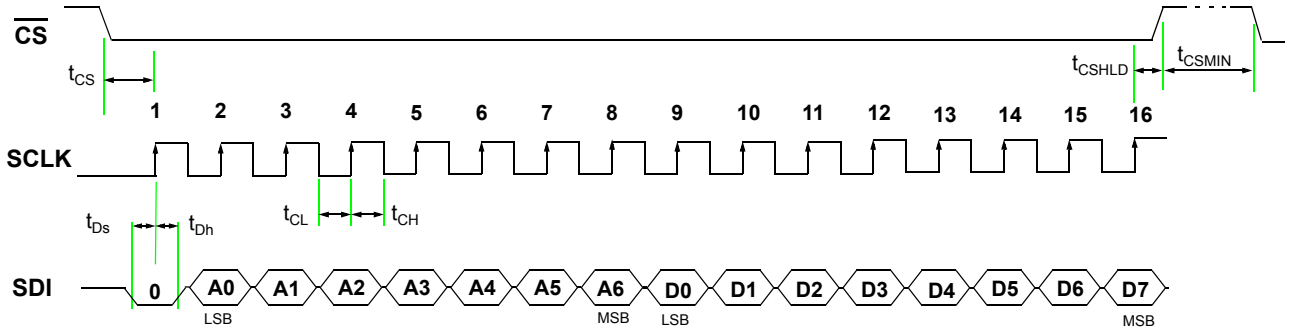


Figure 10:SPI Bus Timing, Write access

Table 7: SPI Bus Timing

Symbol	Description	Min	Max	Unit
t_{CS}	$\overline{CS}$ low to SCLK high	10		ns
t_{CH}	SCLK high time	50		ns
t_{CL}	SCLK low time	50		ns
t_{Ds}	Data setup time	10		ns
t_{Dh}	Data hold time	10		ns
t_{DRDY}	Data ready		7	ns
t_{DHLD}	Data hold	3		ns
t_{CSHLD}	$\overline{CS}$ hold	30		ns
t_{CSTRI}	$\overline{CS}$ off to data tri-state		5	ns
t_{CSMIN}	Minimum delay between successive accesses	50		ns

Motorola Bus Mode

In Motorola mode, the device will interface to 680xx type processors. The $\overline{CS}$, $\overline{WR}$, A(0-6), AD(0-7) and RDY pins are used. Timing is as follows in Figure 11 and Figure 12:

Motorola Bus Timing

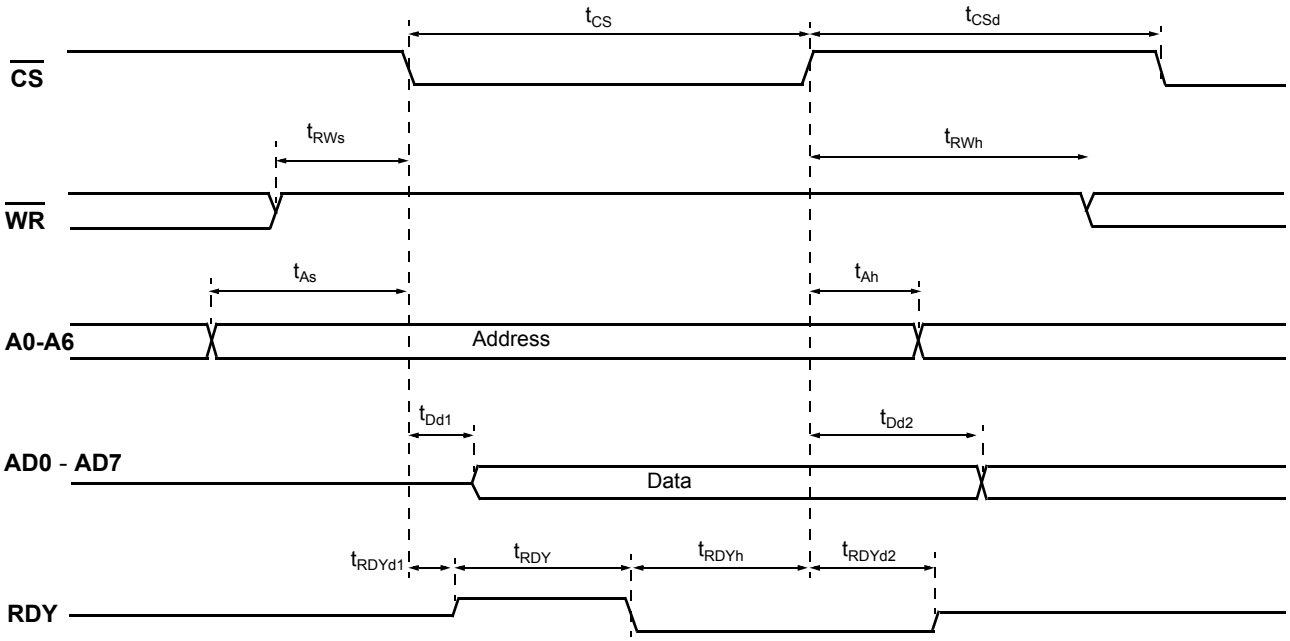


Figure 11: Motorola Bus Read Timing

Table 8: Motorola Bus Read Timing

Symbol	Description	Min	Max	Unit
t_{CS}	$\overline{CS}$ low time	50		ns
t_{CSd}	$\overline{CS}$ minimum high time between reads/writes	50		ns
t_{RWs}	Read/write setup time	0		ns
t_{RWh}	Read/write hold time	0		ns
t_{As}	Address setup	10		ns
t_{Ah}	Address hold	0		ns
t_{Dd1}	Data valid delay from $\overline{CS}$ low		50	ns
t_{Dd2}	Data high-z delay from $\overline{CS}$ high		10	ns
t_{RDYd1}	$\overline{CS}$ low to RDY high delay		13	ns
t_{RDY}	RDY high time	37	50	ns
t_{RDYh}	$\overline{CS}$ hold after RDY low	0		ns
t_{RDYd2}	RDY high-z delay after $\overline{CS}$ high		9	ns

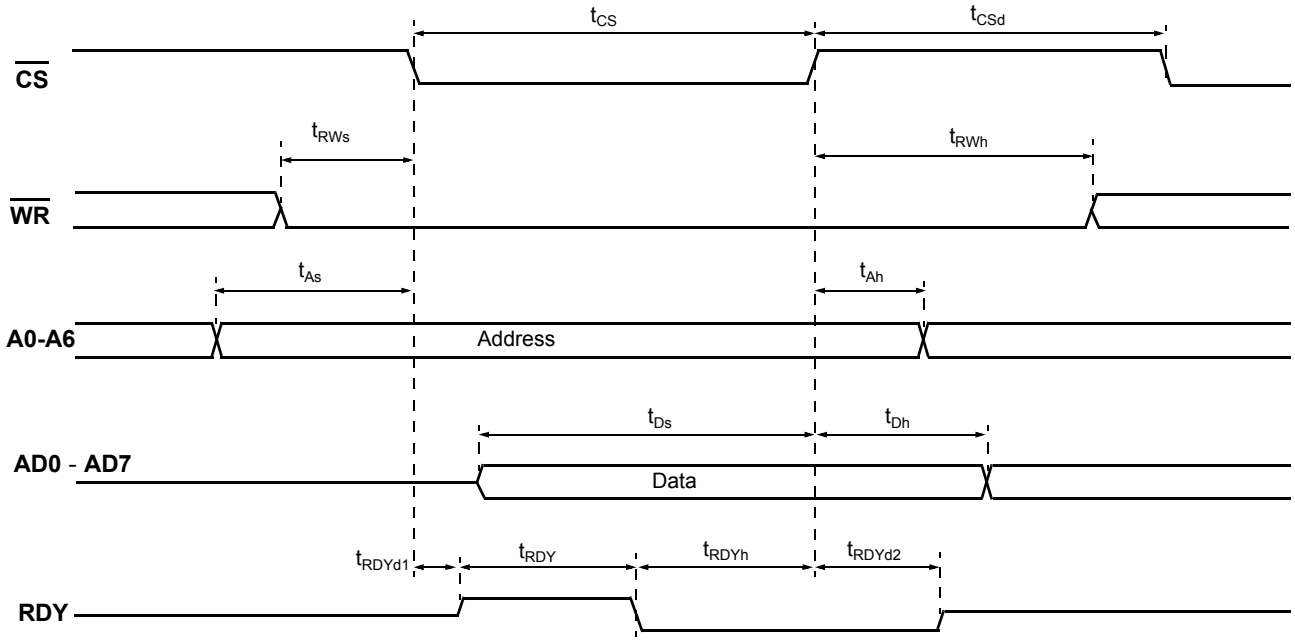


Figure 12: Motorola Bus Write timing

Table 9: Motorola Bus Write Timing

Symbol	Description	Min	Max	Unit
t_{CS}	$\overline{CS}$ low time	50		ns
t_{CSd}	$\overline{CS}$ minimum high time between writes/reads	50		ns
t_{RWs}	Read/write setup time	0		ns
t_{RWh}	Read/write hold time	0		ns
t_{As}	Address setup	10		ns
t_{Ah}	Address hold	0		ns
t_{Ds}	Data setup time before $\overline{CS}$ high	10		ns
t_{Dh}	Data hold time after $\overline{CS}$ high	10		ns
t_{RDYd1}	$\overline{CS}$ low to RDY high delay		13	ns
t_{RDY}	RDY high time	37		ns
t_{RDYh}	$\overline{CS}$ hold after RDY low	0		ns
t_{RDYd2}	RDY high-z delay after $\overline{CS}$ high		7	ns

Intel Bus Mode

In Intel mode, the device will interface to 80x86 type processors. The $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, A(0-6), AD(0-7), and RDY pins are used. Timing is as follows in Figure 13 and Figure 14:

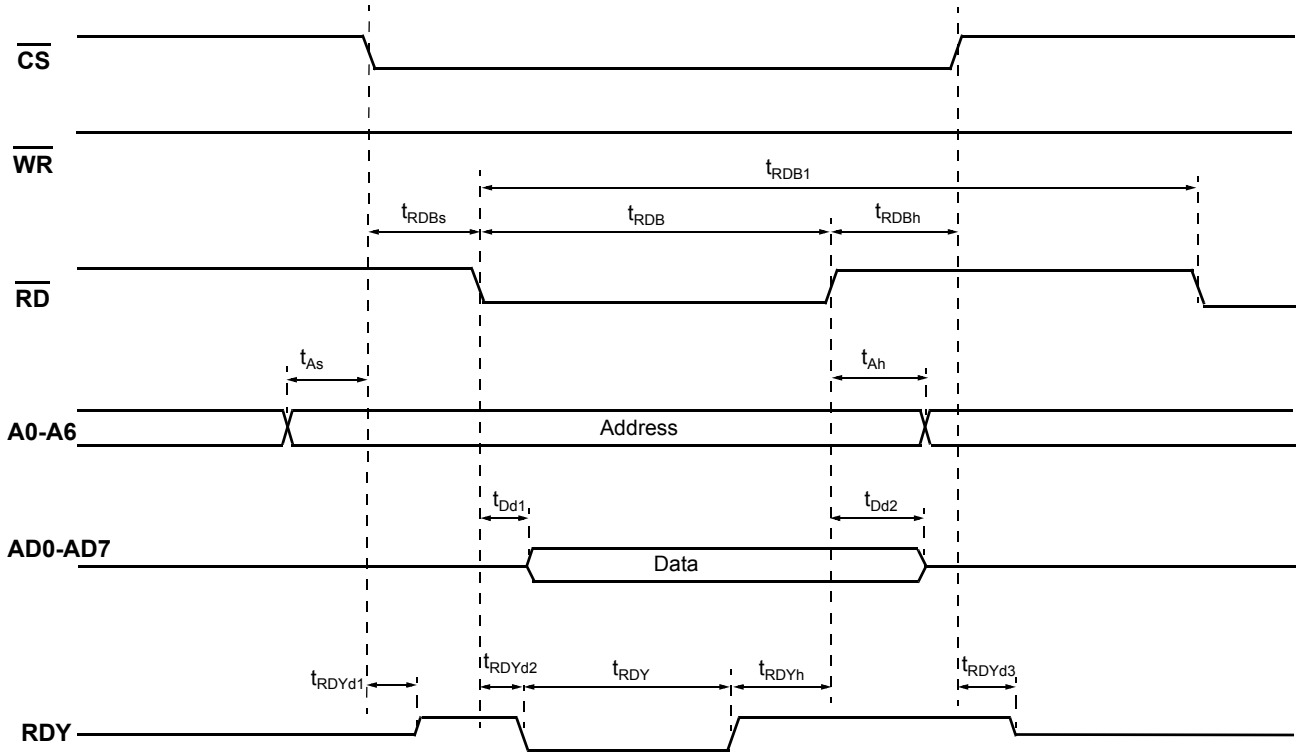


Figure 13: Intel Bus Read Timing

Table 10: Intel Bus Read Timing

Symbol	Description	Min	Max	Unit
t_{RDBs}	Read setup time	0		ns
t_{RDB}	Read low time	40		ns
t_{RDBh}	Read hold time	0		ns
t_{RDB1}	Time between consecutive reads	50		ns
t_{As}	Address setup	10		ns
t_{Ah}	Address hold	0		ns
t_{Dd1}	Data valid delay from RDB low		50	ns
t_{Dd2}	Data high-z delay from RDB high		10	ns
t_{RDYd1}	$\overline{CS}$ low to RDY high delay		13	ns
t_{RDYd2}	$\overline{RD}$ low to RDY low		40	ns
t_{RDY}	RDY low time	50		ns
t_{RDYh}	$\overline{RD}$ hold after RDY high	0		ns
t_{RDYd3}	RDY high-z delay after $\overline{CS}$ high		11	ns

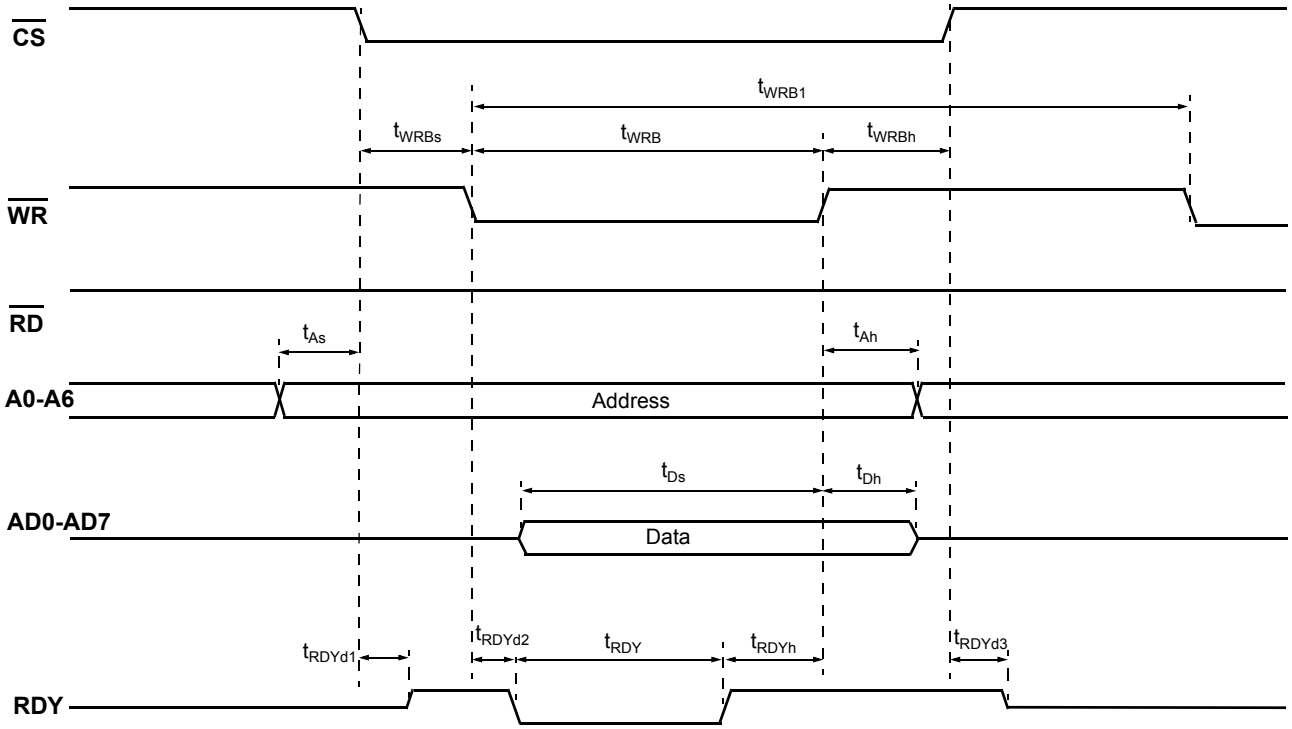


Figure 14: Intel Bus Write Timing

Table 11: Intel Bus Write Timing

Symbol	Description	Min	Max	Unit
t_{WRBs}	Write setup time	0		ns
t_{WRB}	Write low time	40		ns
t_{WRBh}	Write hold time	0		ns
t_{WRB1}	Time between consecutive writes	50		ns
t_{As}	Address setup	10		ns
t_{Ah}	Address hold	0		ns
t_{Ds}	Data setup time before $\overline{WR}$ high	10		ns
t_{Dh}	Data hold time after $\overline{WR}$ high	10		ns
t_{RDYd1}	$\overline{CS}$ low to RDY high delay		13	ns
t_{RDYd2}	$\overline{WR}$ low to RDY low		40	ns
t_{RDY}	RDY low time	50		ns
t_{RDYh}	$\overline{WR}$ hold after RDY high	0		ns
t_{RDYd3}	RDY high-z delay after $\overline{CS}$ high		10	ns

Multiplex Bus Mode

In multiplex bus mode, the device can interface with microprocessors which share the address and data on the same bus signals. The ALE, $\overline{CS}$, WR, $\overline{RD}$, AD(0-7), and RDY pins are used. Timing is as follows in Figure 15 and Figure 16

Multiplex Bus Timing

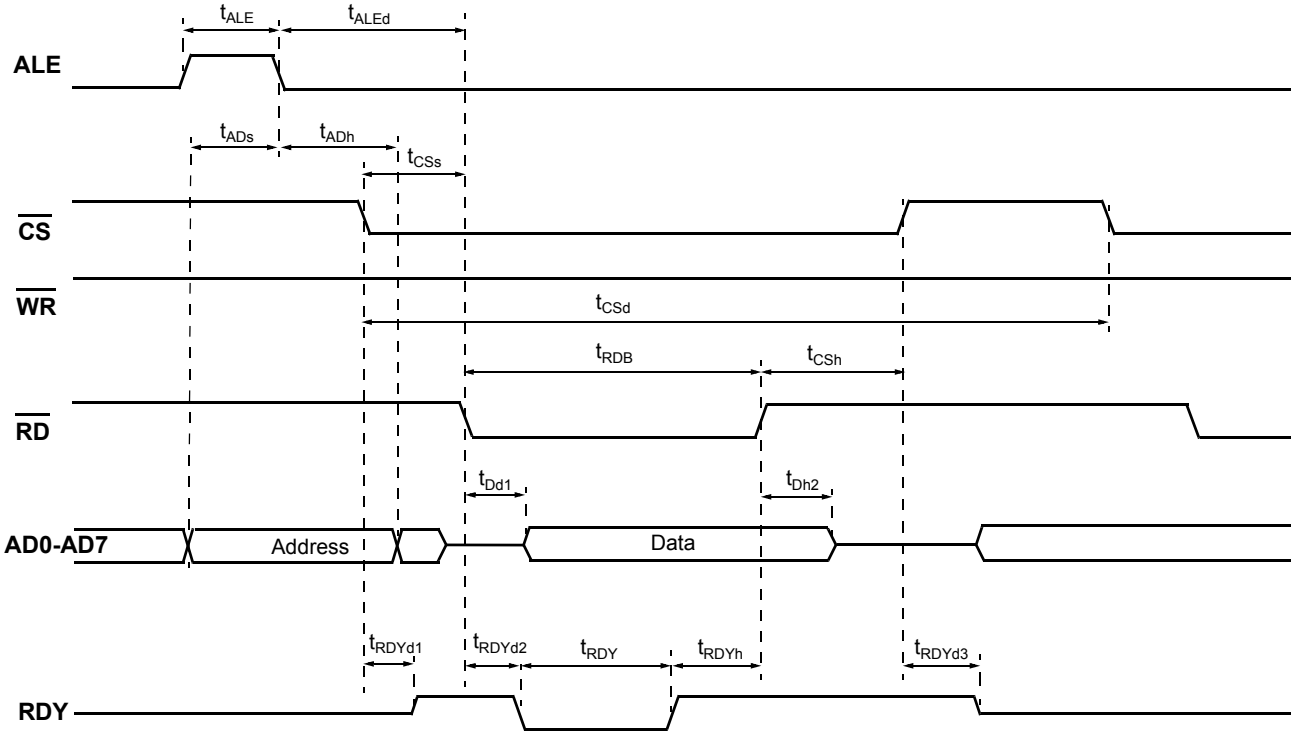


Figure 15: Multiplex Bus Read Timing

Table 12: Multiplex Bus Read Timing

Symbol	Description	Min	Max	Unit
t_{ALE}	ALE high time	10		ns
t_{ALEd}	ALE falling edge to $\overline{RD}$ low	0		ns
t_{ADs}	Address setup time	10		ns
t_{ADh}	Address hold time	10		ns
t_{CSs}	Read setup time	0		ns
t_{RDB}	Read time	40		ns
t_{CSh}	$\overline{CS}$ hold time	0		ns
t_{CSd}	$\overline{CS}$ delay for multiple read/writes	50		ns
t_{Dd1}	Data valid delay from $\overline{RD}$ low		50	ns
t_{Dh2}	Data high-z from $\overline{RD}$ high		10	ns
t_{RDYd1}	$\overline{CS}$ low to RDY active		13	ns
t_{RDYd2}	$\overline{RD}$ low to RDY low		40	ns
t_{RDY}	RDY low time	50		ns
t_{RDYh}	$\overline{RD}$ hold after RDY high	0		ns
t_{RDYd3}	RDY high-z delay after $\overline{CS}$ high		10	ns

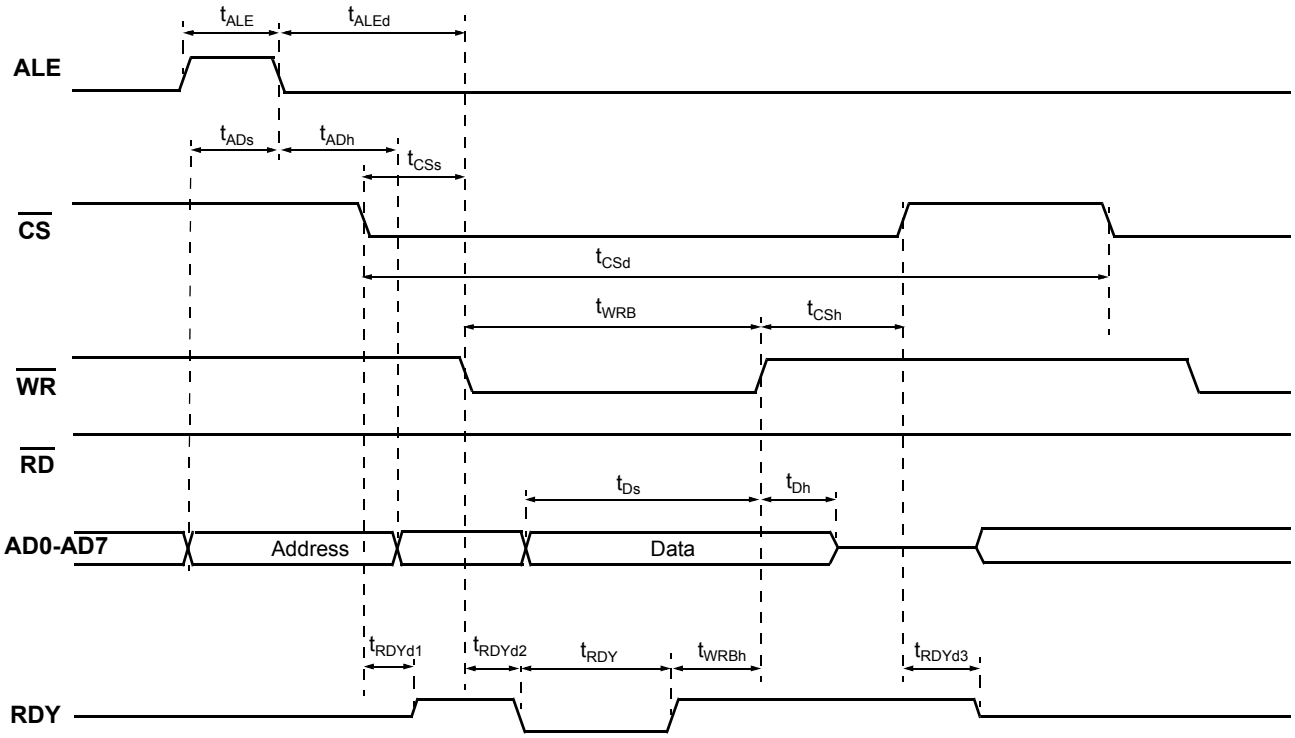


Figure 16: Multiplex Bus Write Timing

Table 13: Multiplex Bus Write Timing

Symbol	Description	Min	Max	Unit
t_{ALE}	ALE high time	10		ns
t_{ALEd}	Time between ALE falling edge and $\overline{WR}$ low	0		ns
t_{ADs}	Address setup time	10		ns
t_{ADh}	Address hold time	10		ns
t_{CSs}	Write $\overline{CS}$ setup time	0		ns
t_{WRB}	Write time	40		ns
t_{CSh}	$\overline{CS}$ hold time	10		ns
t_{CSd}	$\overline{CS}$ delay for multiple write/reads	50		ns
t_{Ds}	Data setup time	10		ns
t_{Dh}	Data hold time	10		ns
t_{RDYd1}	$\overline{CS}$ low to RDY active		13	ns
t_{RDYd2}	$\overline{WR}$ low to RDY low		40	ns
t_{RDY}	RDY low time	50		ns
t_{WRBh}	$\overline{WR}$ hold after RDY high	0		ns
t_{RDYd3}	RDY high-z delay after $\overline{CS}$ high		9	ns

Register Descriptions and Operation

General Register Operation

The STC5420 device has 1, 2, 3, and 4 byte registers. One-byte registers are read and written directly. Multiple -byte registers must be read and written in a specific manner and order, as follows:

Multibyte register reads

A multi byte register read must commence with a read of the least significant byte first. This triggers a latch of the remaining byte(s) to a holding register, ensuring that the remaining data will not change with the continuing operation of the device. The remaining byte(s) must be read consecutively with no intervening read/writes from/to other registers.

Multibyte register writes

A multi byte register write must commence with a write to the least significant byte first. Subsequent writes to the remaining byte(s) must be performed in ascending byte order, consecutively, with no intervening read/ writes from/to other registers, but with no timing restrictions. Multibyte register writes are temporarily stored in a holding register, and are transferred to the target register when the most significant byte is written.

Chip_ID, 0x00 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x00	0x20							
0x01	0x54							

Indicates chip's ID number

Chip_Rev, 0x02 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x02	Revision Number							

Indicates the revision number of STC5420

Chip_Sub_Rev, 0x03 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x03	Sub-Revision Number							

Indicates the firmware revision number of STC5420

T0_MS_Sts, 0x04 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x04	Not used							T0 M/S

Indicates the T0 timing generator operating in master or slave mode.
This state is selected by pin **MC_SL**. *1 = Master, 0 = slave*

T0_Slave_Phase_Adj, 0x05 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x05	Adjust T0 slave phase from -3276.8 to +3276.7ns in 0.1 ns steps							
0x06								

The T0 slave phase may be adjusted from -3276.7 to +3276.7ns, in 0.1 ns steps.

Default value: 0

Fill_Obs_Window, 0x07 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x07	Not used				Leaky bucket fill observation window, *m* = 0 ~ 15			

Sets the fill observation window size for the reference activity monitor to (*m*+1) ms. The window size can be set from 1ms to 16ms.

Default value: *m* = 0, (1ms)

Leak_Obs_Window, 0x08 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x08	Not used				Leaky bucket fill observation window, *n* = 0 ~ 15			

Sets the leak observation window size for the reference activity monitor to (*n* + 1) times the fill observation window size. The size can be set from 1 to 16ms times the fill observation window size.

Default value: *n* = 3, (4 times)

Bucket_Size, 0x09 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x09	Not used		Leaky bucket size, 0 ~ 63					

Sets the leaky bucket size for the reference activity monitor. Bucket size equal to 0 will bypass the leaky bucket accumulator, and assert or de-assert the activity alarm based on results of frequency detector and pulse monitor only.The bucket size must be greater than or equal to the alarm assert value. Otherwise, the value will not be written to the register.

Default value: 20

Assert_Threshold, 0x0A (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0A	Not used		Leaky bucket alarm assert threshold, 1 ~ 63					

Sets the leaky bucket alarm assert threshold for the reference activity monitor. The alarm assert threshold value must be greater than the de-assert threshold value and less than or equal to the bucket size value. Otherwise, the value will not be written to the register.

Default value: 15

De_Assert_Threshold, 0x0B (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0B	Not used		Leaky bucket alarm de-assert threshold, 0 ~ 62					

Sets the leaky bucket alarm de-assert threshold for the reference activity monitor. The de-assert threshold value must be less than the assert threshold value. Otherwise, the value will not be written to the register.

Default value: 10

Freerun_Cali, 0x0C (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0C	Lower 8 bits of Freerun Calibration							
0x0D	Not used					Upper 3 bits of Freerun Calibration		

Freerun calibration, from -102.4 to +102.3 ppm, in 0.1ppm steps, 2's complement.

Default value: 0

Disqualification_Range, 0x0E (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0E	Lower 8 bits of Disqualification Range							
0x0F	Not used						Upper 2 bits Disqualification Range	

Reference disqualification range of fractional frequency offset, from 0 to +102.3 ppm, in 0.1 ppm steps. This also sets the pull-in range. (See the **Reference Input Monitoring and Qualification** section). New disqualification range must be greater than qualification range in register Qualification_Range. Otherwise, the value will not be written to the register.

Default value: 110 (range = 11.0 ppm).

Qualification_Range, 0x10 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x10	Lower 8 bits of Qualification Range							
0x11	Not used						Upper 2 bits Qualification Range	

Reference qualification range of fractional frequency offset, from 0 to +102.3 ppm, in 0.1 ppm steps. New qualification must be less than disqualification range. Otherwise, the value will not be written to the register.

Default value: 100 (range = 10.0 ppm).

Qualification_Soaking_Time, 0x12 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x12	Not used		0 ~ 63 s					

Sets the soaking time for reference qualification, from 0 to 63s, in 1s step.

Default value: 10 (10s)

Ref_Index_Selector, 0x13 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x13	Not used				REF1~REF12			

Select a reference input to access the register **Ref_Info** and **Ref_Acceptable_Freq**.

Valid values from 1 to 12 are relative to Ref1 to Ref12. Invalid values will not be written to the register.

Default value: 1

Ref_Info, 0x14 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x14	Lower 8 bits of frequency offset							
0x15	Reference frequency				Upper 4 bits of frequency offset			

Frequency offset (Bit11~Bit0):

- Indicates the frequency offset the reference input selected by the register **Ref_Index_Selector**. Frequency offset is from -204.7 to +204.7 ppm relative to calibrated freerun clock, in 0.1 ppm steps, 2's complement. A value of -2048 indicates the reference is out of range.

Reference frequency (Bit15~Bit12):

- Indicates frequency of the auto-detect reference input selected by the register **Ref_Index_Selector**. When field value of is 15, means manually acceptable reference input frequency is being used. Refer to the register **Ref_Acceptable_Freq** for the manually acceptable frequency setting.

The reference frequency is determined as follows ("Unknown" indicates a signal is present, but frequency is undetermined):

Field Value	Frequency
0	No signal
1	8 kHz
2	64 kHz
3	1.544 MHz
4	2.048 MHz

Field Value	Frequency
5	19.44 MHz
6	38.88 MHz
7	77.76 MHz
8	6.48MHz
9	8.192MHz
10	16.384MHz
11	25 MHz
12	50 MHz
13	125 MHz
14	Unknown
15	Manually acceptable frequency is used

Refs_Activity, 0x16 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x16	Ref 8	Ref 7	Ref 6	Ref 5	Ref 4	Ref 3	Ref 2	Ref 1
0x17	Not used			Cross ref	Ref 12	Ref 11	Ref 10	Ref 9

Reference activity indicator.
0 = inactive, 1 = active

Refs_Qual, 0x18 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x18	Ref 8	Ref 7	Ref 6	Ref 5	Ref 4	Ref 3	Ref 2	Ref 1
0x19	Not used				Ref 12	Ref 11	Ref 10	Ref 9

Reference qualification indicator.
0 = not qualified, 1 = qualified.

Interrupt_Event_Sts, 0x1A (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1A	Event 7	Event 6	Event 5	Event 4	Event 3	Event 2	Event 1	Event 0

Event 0: Reference qualification status
0 = no change, 1 = reference qualification status changed.
Event1: Cross reference activity status
0 = no change, 1 = cross reference activity status changed.
Event2: T0 selected reference in auto-selection mode
0= no change, 1 = T0 selected reference changed
Event3: T0 PLL status
0= no change, 1 = T0 PLL status changed
Event4: T0 timing generator's event out
0= no event out, 1= any of T0 PLL event out is asserted or not cleared at the register of PLL_Event_Out
Event5: T4 selected reference in auto-selection mode

0= no change, 1 = T4 selected reference changed
Event6: T4 PLL status
0= no change, 1 = T0 PLL status changed
Event7: T4 timing generator's event out
0= no event out, 1= any of T4 PLL event out is asserted or not cleared at the register of PLL_Event_Out

Interrupts are cleared by writing "1" to the bit positions

Default value: 0

Interrupt_Event_Mask, 0x1B (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1B	Event 7	Event 6	Event 5	Event 4	Event 3	Event 2	Event 1	Event 0

Selects which of events will assert the pin EVENT_INTR to active mode (See register **Interrupt_Config**).
0 = mask out, 1 = enable

Default value: 0

Interrupt_Config, 0x1C (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1C	Not used						Idle mode	Active signal level

Active signal level
Sets the signal level in active mode.
0 = active low. 1 = active high

Idle mode
Specify the state of pin EVENT_INTR when no interrupt event occurs.
0 = tri-state. 1 = logic inactive

Default value: 0

Hard_Wired_Switch_Pre_Selection, 0x1D (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1D	Pre-selected reference number 2				Pre-selected reference number 1			

Pre select reference number 1 and reference number 2 in hard-wired manual reference selection mode. This mode is controlled by pin SRCSW. When pin SRCSW is LOW, reference number 1 is pre-selected. When pin SRCSW is HIGH, reference number 2 is pre-selected. It only can be configured when bit7 of Control_Mode register is set to 1 (See register **Control_Mode**).

Field Value	Selection
0	Freerun
1~12	Ref1~Ref12
13	Holdover
14~15	Reserved

Default value: 0

SRCSW_Status, 0x1E (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1E	Not used							Pin status

Indicates status of pin SRCSW.
0 = Low; 1 = High

Default value: 0

T0/T4_Tag_Select, 0x1F (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1F	Not used							Tag_Select

Selects register 0x20 ~ 0x3f mapping to T0 or T4 control mode.
0 = T0; 1 = T4

Default value: 0

Control_Mode, 0x20 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x20	Hard_Wired_Switch	Slave_Inherit_Mode	OOP	Ref_Sel_Mode	Revertive	HO_Usage	Internal Test	

Mode control bits for individual timing generator.

Internal Test
0 = Normal operation; 1 ~3= Reserved

HO_Usage
Determines which holdover history is used.
0 = Device Holdover History (DHH); 1 = User specified history

Revertive
Selects the revertive mode or non-revertive mode of the auto selector.
0 = Non-revertive; 1 = Revertive

Ref_Sel_Mode
Determines reference selection mode.
0 = Manual; 1 = Auto

This bit may be overrided by bit7 of this register.

OOP
In manual mode, when the selected reference is out of the pull-in range, as specified in register **Disqualification_Range** (0x10). OOP will determine if the reference is to be followed,
0 = Follow, 1 = Stop following at pull-in range boundary

Slave_Inherit_Mode
0 = Ignore; 1 = Slave device's auto reference elector will select the reference which master device was locked to when the cross reference is used.

Hard_Wired_Switch (T0 timing generator only)
0 = Not hard-wired Switch, selects reference in manual selection mode or auto selection mode;
1 = Hard-wired Switch, selects reference in hard-wired manual selection mode by using control pin SRCSW to fast manual switch between two pre-selected reference inputs. See register **Hard_Wired_Switch_Pre_Selection**.

Default value: 0

Loop_Bandwidth, 0x21 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x21	Bandwidth select							

Sets each timing generator's loop bandwidth:

Field Value	Bandwidth, Hz
0	103
1	52
2	27
3	13
4	6.7
5	3.4
6	1.7
7	0.84
8	0.42
9	0.21
10	0.10
11~255	Reserved

Default value: 6

Auto_Elect_Ref, 0x22 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x22	Not used				Auto selected reference			

Indicates the auto-elect reference. The auto-elect reference is elected by the elector according to revertivity status, and each reference's priority and qualification. Reference auto-elector keep electing the reference even in manual reference selection mode.

Bit 3 ~ Bit 0	Selection
0	Freerun
1 ~ 12	Sync with Ref 1 ~ Ref 12
13	Holdover
14 ~15	Reserved

Manual_Select_Ref, 0x23 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x23	Not used				Manually selected reference			

Selects the reference in manual reference selection mode.

Bit 3 ~ Bit 0	Selection
0	Freerun
1 ~ 12	Sync with Ref 1 ~ Ref 12
13	Holdover
14	Pseudo-Holdover
15	Reserved (for T0); Lock to T0 (for T4)

The register is read only in hard-wired manual switch mode. It indicates the current reference defined by pin SRCSW and **Hard_Wired_Switch_Pre_Selection**.

Default value: 0

Selected_Ref, 0x24 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x24	Not used				Current selected reference			

Indicates the current selected reference.

Field Value	Current selected reference
0	Freerun
1~12	Sync with Ref 1 ~ Ref 12
13	Holdover
14	Pseudo-Holdover
15	Reserved (for T0); Lock to T0 (for T4)

Device_Holdover_History, 0x25 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x25	Bits 0 - 7 of 32 bit Device Holdover History							
0x26	Bits 8 - 15 of 32 bit Device Holdover History							
0x27	Bits 16 - 23 of 32 bit Device Holdover History							

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x28	Bits 24 - 31 of 32 bit Device Holdover History							

The accumulated device holdover history relative to MCLK. 2's complement. Resolution is $0.745x10^{-3}$ ppb.

Long_Term_Accu_History, 0x29 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x29	Bits 0 - 7 of 32 bit Long Term History							
0x2A	Bits 8 - 15 of 32 bit Long Term History							
0x2B	Bits 16 - 23 of 32 bit Long Term History							
0x2C	Bits 24 - 31 of 32 bit Long Term History							

Long term accumulated history relative to MCLK. 2's complement. Resolution is $0.745x10^{-3}$ ppb.

Short_Term_Accu_History, 0x2D (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x2D	Bits 0 - 7 of 32 bit Short term History							
0x2E	Bits 8 - 15 of 32 bit Short term History							
0x2F	Bits 16 - 23 of 32 bit Short term History							
0x30	Bits 24 - 31 of 32 bit Short term History							

Short term accumulated history relative to MCLK. 2's complement. Resolution is $0.745x10^{-3}$ ppb.

User_Specified_History, 0x31 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x31	Bits 0 - 7 of 32 bit User Holdover History							
0x32	Bits 8 - 15 of 32 bit User Holdover History							
0x33	Bits 16 - 23 of 32 bit User Holdover History							
0x34	Bits 24 - 31 of 32 bit User Holdover History							

User accumulated history relative to MCLK. 2's complement. Resolution is $0.745x10^{-3}$ ppb.

Default value: 0

History_Ramp, 0x35 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x35	Long Term History Accumulator Bandwidth				Short Term History Accumulator Bandwidth		Ramp Control	

History accumulator holdover bandwidth and ramp controls.

Bits 7 ~ 4	Long Term History -3dB Bandwidth
0	4.9 mHz
1	2.5 mHz
2	1.2 mHz
3	0.62 mHz
4	0.31 mHz
5	0.15 mHz
6, 7	Reserved
8	1.3Hz
9	0.64Hz
10	0.32Hz
11	0.16Hz
12	79mHz
13	40mHz
14	20mHz
15	9.9mHz

Bits 3 ~ 2	Short Term History -3dB Bandwidth
0	1.3 Hz
1	0.64 Hz
2	0.32 Hz
3	0.16 Hz

Bits 1 ~ 0	Ramp control
0	No Control
1	1.0 ppm/sec
2	1.5 ppm/sec
3	2.0 ppm/sec

Default value: 27 (1.2mHz; 0.64Hz; 2ppm/sec)

Ref_Priority_Table, 0x36 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x36	Ref 2 Priority				Ref 1 Priority			
0x37	Ref 4 Priority				Ref 3 Priority			
0x38	Ref 6 Priority				Ref 5 Priority			
0x39	Ref 8 Priority				Ref 7 Priority			
0x3A	Ref 10 Priority				Ref 9 Priority			
0x3B	Ref 12 Priority				Ref 11 Priority			

Reference priority for automatic reference selector. Lower values have higher priority:

Bits 7~4/Bits 3~0	Reference Priority
0	Revoke from auto reference elector
1 ~ 15	Value 1 ~ 15

Default value: 0

PLL_Status, 0x3C (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x3C	HHA	DHT	FEE	SAP	OOP	LOL	LOS	SYNC

SYNC Indicates synchronization has been achieved
0 = Not synchronized
1 = Synchronized

LOS Loss of signal of the selected reference
0 = No Loss
1 = Loss (Indicate loss of signal, freerun, pseudo holdover and holdover)

LOL Loss of lock (Failure to achieve or maintain lock)
0 = No loss of lock
1 = Loss of lock (Indicate loss of lock, freerun, pseudo holdover and holdover)

OOP Out of pull-in range. Indicate the frequency offset of the selected reference input is out of pull-in range.
1 = Out of pull-in range
0 = In range

SAP Indicates the output clocks have stopped following the selected reference, caused by out of pull-in range
1 = Stop following at pull-in range boundary
0 = Following

FEE Frame edge error. Indicates whether an error occurs in the frame edge selection process in slave mode or master phase align mode. For timing generator T0 only.
1 = Frame edge error occurs
0 = No frame edge error occurs

DHT Device Holdover History tracking
1 = Device holdover history is being tracked.
0 = Device holdover history is based on the last available history.

HHA Holdover History Availability. Config **Control_Mode** register to select which of holdover history is used.

Device Holdover History or User Specified History.
1 = Available
0 = Not available

Holdover_Accu_Flush, 0x3D (W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x3D	Not used							HO flush

Writing to this register will perform a flush of the accumulated history. The value of bit zero determines which histories are flushed.

HO flush:

0 = Flush and reset long term history to 0
1 = Flush/reset both long term history and the device holdover history to 0.

PLL_Event_Out, 0x3E (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x3E	Event7	Event6	Event5	Event4	Event3	Event2	Event1	Event0

Event0: Reserved
Event1: Reserved
Event2: Reserved
Event3: Reserved
Event4: Reserved
Event5: Reserved
Event6: Reserved
Event7: Reserved

Events are cleared by writing “1” to the bit positions

PLL_Event_In, 0x3F (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x3F	Event7	Event6	Event5	Event4	Event3	Event2	Event1	Event0

Writing 1 to trigger the event. If the event is acknowledged by the STC5420, event bit is cleared to be 0.

Event0: Relock
Sets PLL to relock the selected reference input. If the device operates in phase-align mode, PLL rese lects the frame edge, relocks and frame phase align to the reference input. If the device operates in non phase-align mode, PLL relocks to the reference input and restart phase rebuild process.
Event1: Reserved
Event2: Reserved
Event3: Reserved
Event4: Reserved
Event5: Reserved
Event6: Reserved
Event7: Reserved

Default value: 0

EX_SYNC_Edge_Config, 0x40 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x40	Not used							Edge Select

Select whether falling edge or rising edge is used as frame reference pulse, when receiving the external frame reference input at pin EX_SYNC.

Bits 0	Edge Select
0	Falling edge
1	Rising edge

Default value: 1

Slave_Frame_Align, 0x41 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x41	Not used				Frame Edge Select		Cross Ref Source and Frame Ref Select	

Selects the cross reference source and sampling edge of cross reference for T0 frame alignment in slave mode. T4 timing generator not support slave mode.

Cross Ref Source Select: Selects the cross reference and frame reference.

Bits 1 ~ 0	Cross Ref Source and Frame Ref Select
0	Selects high frequency input at pin REF7 as cross reference; Selects 8kHz or 2kHz clock at pin EX_SYNC as external frame reference.
1	Selects 8kHz clock at pin EX_SYNC as cross reference
2	Selects composite signal which contains both cross reference and 2kHz frame information at pin REF7
3	Selects composite signal which contains both cross reference and 2kHz frame information at pin EX_SYNC

Frame Edge Select: Select frame edge of the cross reference if the external frame reference is being used.

Bits 3 ~ 2	Frame Edge Select
0, 1	Selects cross reference's rising edge ***nearest*** to the frame pulse on the external frame reference
2	Selects cross reference's rising edge ***previous*** to the frame pulse on the external frame reference
3	Selects cross reference's rising edge ***next*** to the frame pulse on the external frame reference

Default value: 0

Master_Frame_Align, 0x42 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x42	Frame Phase Alignment and Edge Selection for Ref2		Frame Reference Selection for Ref2		Frame Phase Alignment and Edge Selection for Ref1		Frame Reference Selection for Ref1	
0x43	Frame Phase Alignment and Edge Selection for Ref4		Frame Reference Selection for Ref4		Frame Phase Alignment and Edge Selection for Ref3		Frame Reference Selection for Ref3	
0x44	Frame Phase Alignment and Edge Selection for Ref6		Frame Reference Selection for Ref6		Frame Phase Alignment and Edge Selection for Ref5		Frame Reference Selection for Ref5	
0x45	Frame Phase Alignment and Edge Selection for Ref8		Frame Reference Selection for Ref8		Frame Phase Alignment and Edge Selection for Ref7		Frame Reference Selection for Ref7	
0x46	Frame Phase Alignment and Edge Selection for Ref10		Frame Reference Selection for Ref10		Frame Phase Alignment and Edge Selection for Ref9		Frame Reference Selection for Ref9	
0x47	Frame Phase Alignment and Edge Selection for Ref12		Frame Reference Selection for Ref12		Frame Phase Alignment and Edge Selection for Ref11		Frame Reference Selection for Ref11	

Selects frame reference and sampling edge on selected reference for T0 frame alignment in master mode. T4 timing generator not support frame phase alignment.

Frame Reference Selection:

Bits 1 ~ 0 Bits 5 ~ 4	Frame Reference Select
0	Selects unit's own Frame8K as frame reference
1, 2, 3	Selects 8kHz clock at pin EX_SYNC as external frame reference

Frame phase alignment and edge selection:

Bits 3 ~ 2 Bits 7 ~ 6	Frame Edge Select
0	Frame phase arbitrary mode. Frame reference ignored
1	Frame phase align mode, selects selected reference's rising edge ***nearest*** to the frame pulse on the external frame reference
2	Frame phase align mode, selects selected reference's rising edge ***previous*** to the frame pulse on the external frame reference

Bits 3 ~ 2 Bits 7 ~ 6	Frame Edge Select
3	Frame phase align mode, selects selected reference's rising edge ***next*** to the frame pulse on the external frame reference

Default value: 0

Synth_Index_Select, 0x4A (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x4A	Not Used				Synthesizer index selection for synthesizer frequency and phase skew adjustment			

Determines which synthesizer is selected for setting frequency value at the register **Synth_Freq_Value** and adjusting phase skew at the register **Synth_Skew_Adj.**

CLK1~CLK8 can be derived from synthesizer G_1~G_8 through T0 path, respectively, in which CLK3~CLK8 can also be derived from synthesizer F through T0 path or synthesizer G_{T4} through T4 path.

Field Value	Synthesizer	Associated CLK Output
0	Synthesizer F	CLK8K, CLK2K, CLK3~CLK8
1	Synthesizer G_1	CLK1
2	Synthesizer G_2	CLK2
3	Synthesizer G_3	CLK3
4	Synthesizer G_4	CLK4
5	Synthesizer G_5	CLK5
6	Synthesizer G_6	CLK6
7	Synthesizer G_7	CLK7
8	Synthesizer G_8	CLK8
9	Synthesizer G_{T4}	CLK3~CLK8

Default value: 0

Synth_Freq_Value 0x4B (R/W**)**

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x4B	Bits 0-7 of 18 bits Synthesizer Frequency Selection							
0x4C	Bits 15-8 of 18 bits Synthesizer Frequency Selection							
0x4D	Not used						Bits 17-16 of 18 bits Synthesizer Frequency Selection	

Selects synthesizer frequency value from 1MHz to 156.25MHz, in 1kHz steps, for synthesizer G_1~G_8, or G_{T4}. Synthesizer is selected at register **Synth_Index_Select**. CLK1~CLK8 is derived from synthesizer G_1~G_8 through T0 path, respectively, in which CLK3~CLK8 can also be derived from synthesizer F through T0 path or synthesizer G_{T4} through T4 path.

This reigster is not writable for synthesizer F since its frequency is fixed at 8kHz and 2kHz. But phase skew of synthesizer F is programmable at the register **Synt_Skew_Select.**

Default value varies with synthesizer index selection at the register **Synth_Index_Select**, refer to table below:

Synthesizer Index Selection	Associated CLK Output	Default Value
Synthesizer G_1	CLK1	155520 (155.52MHz)
Synthesizer G_2	CLK2	125000 (125MHz)
Synthesizer G_3	CLK3	19440 (19.44MHz)
Synthesizer G_4	CLK4	38880 (38.88MHz)
Synthesizer G_5	CLK5	2048 (2.048MHz)
Synthesizer G_6	CLK6	25000 (25MHz)
Synthesizer G_7	CLK7	50000 (50MHz)
Synthesizer G_8	CLK8	1544 (1.544MHz)
Synthesizer G_{T4}	CLK3~CLK8	2048 (2.048MHz)

Synth_Skew_Adj, 0x4E (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x4E	Lower 8 bits of Synthesizer Phase Skew Adjustment							
0x4F	Not used				Higher 4 bits of Synthesizer Phase Skew Adjustment			

Phase skew adjust for synthesizers based on which synthesizer index is selected at the register **Synth_Index_Select**. See description of the register **Synth_Index_Select**. The adjustment is from -6400/128 ns to 6396.875/128 ns, which is -50ns ~ 49.976 ns, in 3.125/128 ns steps, 2's complement.

Synthesizer Index Selection	Associated CLK Output
Synthesizer F	CLK8K, CLK2K, CLK3~CLK8
Synthesizer G_1	CLK1
Synthesizer G_2	CLK2
Synthesizer G_3	CLK3
Synthesizer G_4	CLK4
Synthesizer G_5	CLK5
Synthesizer G_6	CLK6
Synthesizer G_7	CLK7
Synthesizer G_8	CLK8
Synthesizer G_{T4}	CLK3~CLK8

Default value: 0 (For all the synthesizers)

CLK1/2_Signal_Level 0x50 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x50	Not used						CLK2 Signal Level	CLK1 Signal Level

Selects the signal level for clock outputs CLK1 and CLK2.
0 = LVPECL, 1 = LVDS

Default value: 0

CLK1_Sel, 0x51(R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x51	Not used						CLK1 Synthesizer Select	

Selects clock output CLK1 derived from synthesizer G_1 or put in tri-state.

Bits 1 ~ 0	CLK1 Synthesizer Select
0, 2, 3	Put CLK1 in tri-state mode
1	Synthesizer G_1

Default value: 0

CLK2_Sel, 0x52(R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x52	Not used						CLK2 Synthesizer Select	

Selects clock output CLK2 derived from synthesizer G_2 or put in tri-state.

Bits 1 ~ 0	CLK2 Synthesizer Select
0, 2, 3	Put CLK2 in tri-state mode
1	Synthesizer G_2

Default value: 0

CLK3_Sel, 0x53 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x53	Not used						CLK3 Synthesizer Select	

Selects the clock output CLK3 derived from synthesizer G_3 (T0), synthesizer F or synthesizer G_{T4} (T4). Composite signal, Frame8K, and Frame2K are all produced at synthesizer F. When synthesizer F is selected, sets bit1~bit0 of the register **Frame_Mux** to select frame pulse clock from composite signal, Frame8K, or Frame2K. Signal level of CLK3 is LVCMOS.

Register Frame_Mux (Bit1~Bit0)	Register CLK3_Sel (Bit1~Bit0)	CLK3 Synthesizer Select
X	0	Put CLK3 in tri-state mode
X	1	Synthesizer G_3 (T0)
0	2	Synthesizer F composite signal (T0)

Register Frame_Mux (Bit1~Bit0)	Register CLK3_Sel (Bit1~Bit0)	CLK3 Synthesizer Select
1	2	Synthesizer F Frame8K
2	2	Synthesizer F Frame2K
3	2	CLK3 tie to ground
X	3	Synthesizer G_{T4} (T4)

Default value: 0

CLK4_Sel, 0x54 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x54	Not used						CLK4 Synthesizer Select	

Selects the clock output CLK4 derived from synthesizer G_4 (T0), synthesizer F or synthesizer G_{T4} (T4). Composite signal, Frame8K, and Frame2K are all produced at synthesizer F. When synthesizer F is selected, sets bit3~bit2 of the register **Frame_Mux** to select frame pulse clock from composite signal, Frame8K, or Frame2K. Signal level of CLK4 is LVCMOS.

Register Frame_Mux (Bit3~Bit2)	Register CLK4_Sel (Bit1~Bit0)	CLK4 Synthesizer Select
X	0	Put CLK4 in tri-state mode
X	1	Synthesizer G_4 (T0)
0	2	Synthesizer F composite signal (T0)
1	2	Synthesizer F Frame8K
2	2	Synthesizer F Frame2K
3	2	CLK4 tie to ground
X	3	Synthesizer G_{T4} (T4)

Default value: 0

CLK5_Sel, 0x55 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x55	Not used						CLK5 Synthesizer Select	

Selects the clock output CLK5 derived from synthesizer G_5 (T0), synthesizer F or synthesizer G_{T4} (T4). Composite signal, Frame8K, and Frame2K are all produced at synthesizer F. When synthesizer F is selected, sets bit5~bit4 of the register **Frame_Mux** to select frame pulse clock from composite signal, Frame8K, or Frame2K. Signal level of CLK5 is LVCMOS.

Register Frame_Mux (Bit5~Bit4)	Register CLK5_Sel (Bit1~Bit0)	CLK5 Synthesizer Select
X	0	Put CLK5 in tri-state mode

Register Frame_Mux (Bit5~Bit4)	Register CLK5_Sel (Bit1~Bit0)	CLK5 Synthesizer Select
X	1	Synthesizer G_4 (T0)
0	2	Synthesizer F composite signal (T0)
1	2	Synthesizer F Frame8K
2	2	Synthesizer F Frame2K
3	2	CLK5 tie to ground
X	3	Synthesizer G_{T4} (T4)

Default value: 0

CLK6_Sel, 0x56 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x56	Not used						CLK6 Synthesizer Select	

Selects the clock output CLK6 derived from synthesizer G_6 (T0), synthesizer F or synthesizer G_{T4} (T4). Composite signal, Frame8K, and Frame2K are all produced at synthesizer F. When synthesizer F is selected, sets bit7~bit6 of the register **Frame_Mux** to select frame pulse clock from composite signal, Frame8K, or Frame2K. Signal level of CLK6 is LVCMOS.

Register Frame_Mux (Bit7~Bit6)	Register CLK6_Sel (Bit1~Bit0)	CLK6 Synthesizer Select
X	0	Put CLK6 in tri-state mode
X	1	Synthesizer G_4 (T0)
0	2	Synthesizer F composite signal (T0)
1	2	Synthesizer F Frame8K
2	2	Synthesizer F Frame2K
3	2	CLK6 tie to ground
X	3	Synthesizer G_{T4} (T4)

Default value: 0

CLK7_Sel, 0x57 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x57	Not used						CLK7 Synthesizer Select	

Selects the clock output CLK7 derived from synthesizer G_7 (T0), synthesizer F or synthesizer G_{T4} (T4). Composite signal, Frame8K, and Frame2K are all produced at synthesizer F. When synthesizer F is selected, sets bit9~bit8 of the register **Frame_Mux** to select frame pulse clock from composite signal, Frame8K, or Frame2K. Signal level of CLK7 is LVCMOS.

Register Frame_Mux (Bit9~Bit8)	Register CLK7_Sel (Bit1~Bit0)	CLK7 Synthesizer Select
X	0	Put CLK7 in tri-state mode
X	1	Synthesizer G_4 (T0)
0	2	Synthesizer F composite signal (T0)
1	2	Synthesizer F Frame8K
2	2	Synthesizer F Frame2K
3	2	CLK7 tie to ground
X	3	Synthesizer G_{T4} (T4)

Default value: 0

CLK8_Sel, 0x58 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x58	Not used						CLK8 Synthesizer Select	

Selects the clock output CLK8 derived from synthesizer G_8 (T0), synthesizer F or synthesizer G_{T4} (T4). Composite signal, Frame8K, and Frame2K are all produced at synthesizer F. When synthesizer F is selected, sets bit11~bit10 of the register **Frame_Mux** to select frame pulse clock from composite signal, Frame8K, or Frame2K. Signal level of CLK8 is LVCMOS.

Register Frame_Mux (Bit11~Bit10)	Register CLK8_Sel (Bit1~Bit0)	CLK8 Synthesizer Select
X	0	Put CLK8 in tri-state mode
X	1	Synthesizer G_4 (T0)
0	2	Synthesizer F composite signal (T0)
1	2	Synthesizer F Frame8K
2	2	Synthesizer F Frame2K
3	2	CLK8 tie to ground
X	3	Synthesizer G_{T4} (T4)

Default value: 0

Frame8K_Sel, 0x59 (R/W)
Frame2K_Sel, 0x5A (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x59		Invert	Duty Cycle Select for Frame8K or put CLK8K into tri-state					
0x5A		Invert	Duty Cycle Select for Frame2K or put CLK2K into tri-state					

Selects duty cycle of the Frame8K and Frame2K generated from synthesizer F and determine frame edge is rising or falling. Set 0 Bit5~0 to put CLK8K/CLK2K into tri-state or put Frame8K/Frame2K of synthesizer F to ground.

Bit 5 ~ 0	Duty Cycle Select
0	Put CLK8K/CLK2K into tri-state or put Frame8K/Frame2K to ground
1~62	Pulse width 1 to 62 cycle of 155.52MHz
63	50% duty cycle

Bits 6	Invert
0	Not inverted (frame on rising edge)
1	Inverted (frame on falling edge)

Default value: 63 (50% duty cycle, not inverted)

Ref_Acceptable_Freq, 0x5B (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x5B	Lower 8 bits of integer N Select							
0x5C	Not used	Higher 7 bits of integer N Select						

Enable frequency auto detect function or set integer N for the manual acceptable reference frequency for individual reference input .

Setting this register to 0 to enable the automatic detection for reference input which is selected at the register **Ref_Index_Selector**. The auto-detect acceptable reference input frequencies are shown in Table 3.

Select the integer N for the manually acceptable reference at frequency of Nx8kHz (N is integer from 1 to 32767) for REF1 ~ REF12. Which of reference input is selected for the manually acceptable reference is depending on the index selected at the register **Ref_Index_Selector**.

Setting integer N (from 1 to 32767) at this register allows user to manually select the acceptable reference input frequency at the integer multiple of 8kHz, range from 8kHz to 262.136MHz. For instance, user can select integer N = 19440 to manually accept frequency at 19440x8kHz = 155.52MHz.

Field Value	Integer N Select
0	Enable auto detection for reference input
1~32767	Integer N for the manual acceptable reference frequency

Default value: 0

Frame_Mux, 0x5D (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x5D	Frame mux of CLK6 selection		Frame mux of CLK5 selection		Frame mux of CLK4 selection		Frame mux of CLK3 selection	
0x5E	Not used				Frame mux of CLK8 selection		Frame mux of CLK7 selection	

Select one of frame signals (Frame8K, Frame2K, and composite signal) derived from synthesizer F and forward it to output selection of CLK3~CLK8 individually. Output selection of CLK3~CLK8 is programmed at the registers **CLK(3~8)_Sel**.

Bit1~Bit0 Bit3~Bit2 Bit5~Bit4 Bit7~Bit6 Bit9~Bit8 Bit11~Bit10	Frame signal select
0	Proprietary composite signal
1	Frame8K
2	Frame2K
3	Ground

Default value: 0

Diff_REF_Polarity, 0x5F (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x5F	Not used						REF12 Polarity	REF11 Polarity

Reverse polarity of positive and negative for differential reference input REF11_P/REF11_N and REF12_P/REF12_N.

REF11/REF12 Polarity:
1: Normal polarity
0: Reverse polarity of P and N. Use falling edge of P instead of rising edge

Default value: 3

Field_Upgrade_Status, 0x70 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x70	Not used					Load_Complete	READY	Checksum

Checksum
Checks whether the 7600 bytes firmware configuration data is loaded successfully.
0 = Fail, 1 = Success

READY
Indicates if field upgrade is ready to begin, normally is set to 1 at 3 milliseconds (3ms) after the reset.
0 = Not ready
1 = Ready

Load_Complete
Indicates whether the loading of 7600 bytes firmware configuration data is complete.
0 = Not complete
1 = Complete

Field_Upgrade_Data, 0x71 (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x71	Field upgrade of firmware configuration data							

Writes the firmware configuration data (7600 bytes) to this register one byte at a time to complete data loading. Only the last written byte can be read from this register, no matter how many times of reads performed.

Default value: 0

Field_Upgrade_Count, 0x72 (R)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x72	Lower 8 bits of byte count for firmware configuration data							
0x73				Higher 5 bits of byte count for firmware configuration data				

Reads this register for how many bytes of 7600 bytes firmware configuration data has been loaded through the register **Field_Upgrade_Data** (0x71).

Default value: 0

Field_Upgrade_Start, 0x74 (W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x74	Start field upgrade							

If bit READY of the register **Field Upgrade Status** (0x70) is set to 1, user can write three values to this register consecutively, with no intervening read/writes from/to other registers to start the process of field upgrade. 7600 bytes firmware configuration data can only start loading after the three values are written successfully.

Sequence of Writes	Bit 7 ~ 0
First	0x51
Second	0x52
Third	0x53

MCLK_Freq_Reset, 0x7F (R/W)

Register Writes:

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x7F	External oscillator frequency selection							

Select accepted frequency of MCLK input by writing the associated value to this register three times consecutively, with no intervening read/writes from/to other register. The associated values for the four accepted frequency (10MHz, 12.8MHz, 19.2MHz, 20MHz) are as shown in table below. Three times of consecutive writes will trigger internal soft-reset. Initial default accepted frequency for STC5420 is 12.8MHz. The accepted fre-

quency of MCLK input returns to 12.8MHz following any regular reset.

Perform writes at least 50us after the regular reset has done.

Associated written values are shown below:

Bit 7 ~ 0	External Oscillator Frequency Selection
0x11	10MHz
0x22	12.8MHz
0x44	19.2MHz
0x88	20MHz

Register Read:

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x7F	FRQID		COUNT		ID_Written_Value			

This register allows the user read back three values as follows:

FRQID
Indicates the ID of the frequency of MCLK that the STC5420 currently accept. Constant 1 can be read from FRQID initially since the default accepted frequency for the STC5420 is 12.8MHz. The value of FRQID can only be updated when three consecutive valid writes are written to the register **MCLK_Freq_Reset** completely.

Bit 7 ~ 6 FRQID	MCLK Frequency
0	10MHz
1	12.8MHz
2	19.2MHz
3	20MHz

COUNT
Indicates how many times this register has been written to. COUNT is set to 1 when each time a different valid associated value is written to for the first time and is clear to 0 after three times valid writes are completed.

As described above in Register Writes, the associated value should be written to this register three times consecutively, with no intervening read/writes from/to other register. If the written value is invalid or the consecutive writes operation is interrupted by reading/writing from/to other register, COUNT is clear to 0.

Bit 5 ~ 4 COUNT	Counter
0	No written or invalid
1	Once
2	Twice
3	Three times

ID_Written_Value

Indicates the ID of associated value that is being written to this register. The ID is updated when each time a different valid associated value is written to this register for the first time.

As described above in Register Writes, the associated value should be written to this register three times consecutively, with no intervening read/writes from/to other register. If the written value is invalid or the consecutive writes operation is interrupted by reading/writing from/to other register, ID_Written_Value is clear to 0.

Bit 3 ~ 0 ID_Written_Value	Written value to this register (0x7F)
0	No written or invalid
1	0x11
2	0x22
4	0x44
8	0x88

Default value: 0x40 (12.8MHz)

Noise Transfer Functions

User may write to register **Loop Bandwidth** to set the PLL loop bandwidth for each timing generator. The noise transfer function of the PLL filter is determined by the loop bandwidth. Figure 17 shows the noise transfer functions as the loop bandwidth vary from 100mHz to 103Hz.

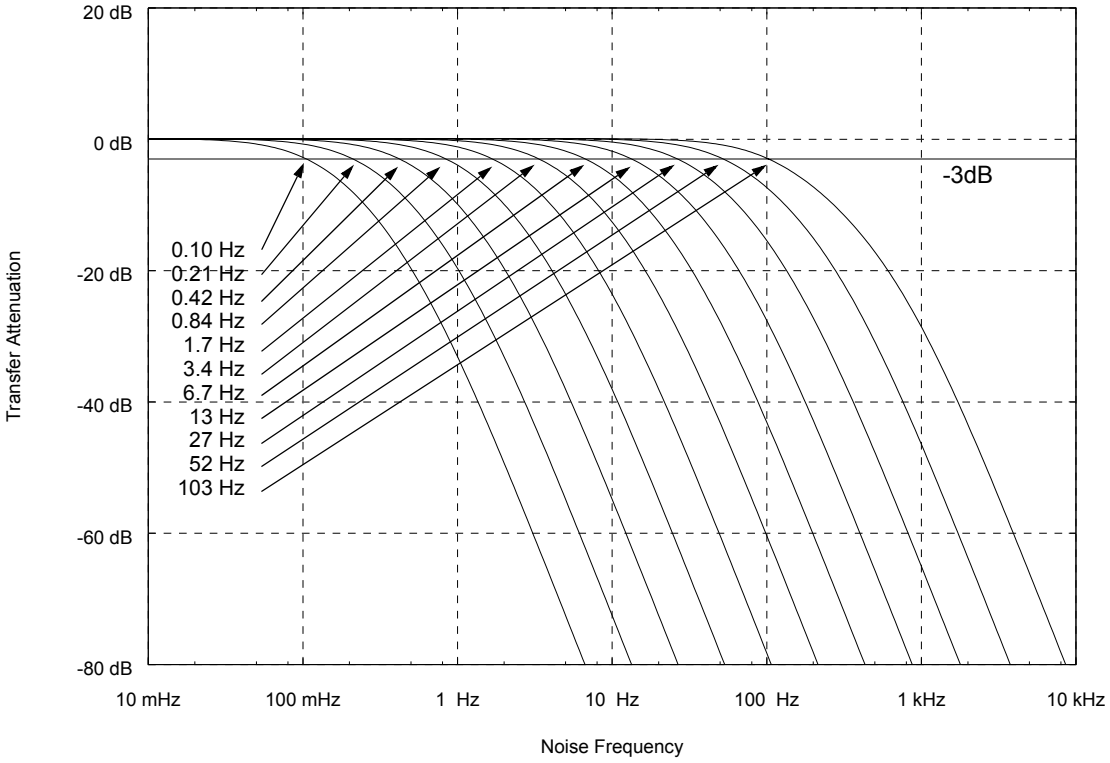


Figure 17: Noise Transfer Functions

Order Information

All STC5420 parts are RoHS 6/6 compliant. The product revision number is provided by register Chip_Rev (0x02) and Chip_Sub_Rev (0x03). The revision number has format of A.B.C. The latest revision is 3.1.1. It is backward compatible with previous revisions. Distribution of the register address is shown below:

Chip_Rev

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x02	A				B			

Chip_Sub_Rev

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x03	C							

Part Number	Description
STC5420 rev 3.1.1	Industrial Temperature Range Model (-40°C ~ +85 °C)

Specification Modification

This section lists the changes to STC5420 specification from previous revision 2.01. Current revision is STC5420 rev 3.1.1.

- Add a frame mux to allow user to select Frame8K or Frame2K for clock output CLK3~CLK8 individually. See register **Frame_Mux** and **CLK(3~8)_Sel**.
- Add a register to reverse polarity of differential reference input REF11_P/REF11_N and REF12_P/ REF12_N. See register **Diff_REF_Polarity**.
- Remove LVCMOS level for REF11 and REF12

Application Notes

This section describes typical application use of the STC5420 device. The General section applies to all application variations.

General

Power and Ground

Well-planned noise-minimizing power and ground are essential to achieving the best performance of the device. The device requires 3.3V digital power and analog power input.

It is desirable to provide individual 0.1uF bypass capacitors, located close to the chip, for each of the power input leads, subject to board space and layout constraints.

Ground should be provided by as continuous a ground plane as possible. A separated analog ground plane is recommended.

Note: Un-used reference inputs must be grounded.

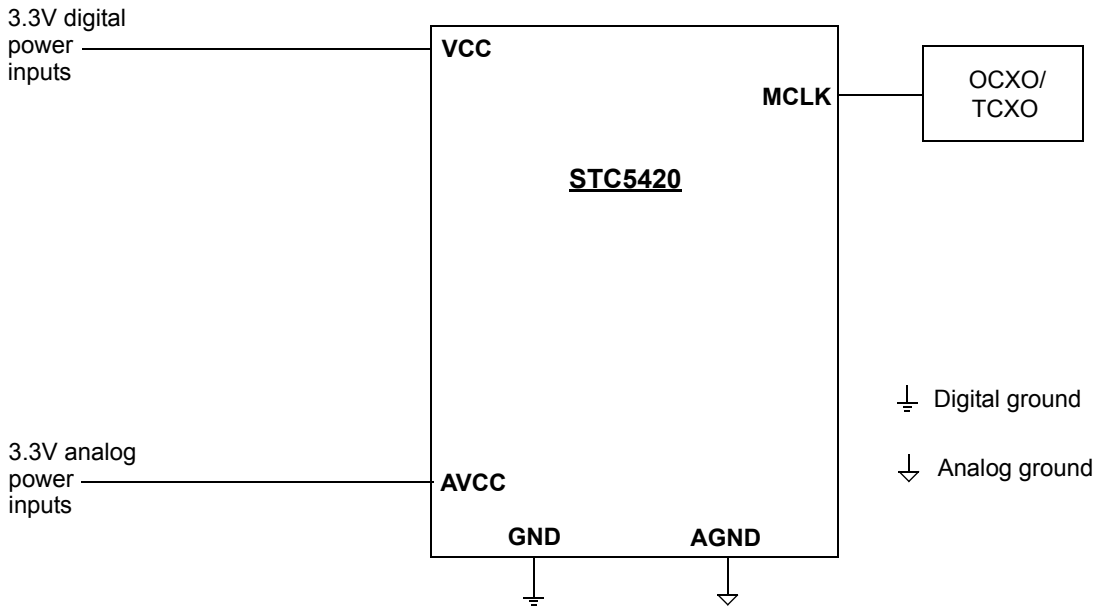
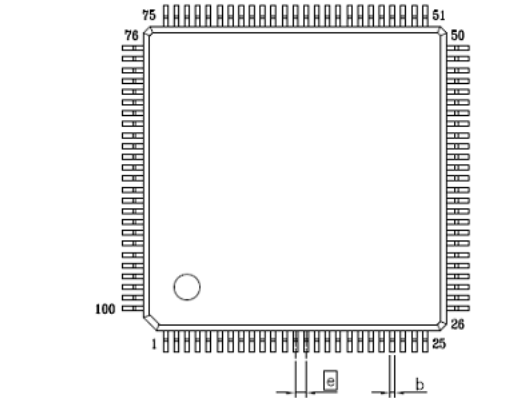


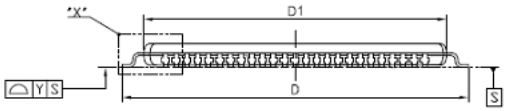
Figure 18: Power and Ground

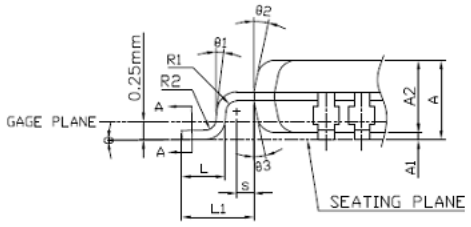
Master Oscillator

An external 3.3V LVCMOS level clock (generally derived from TCXO or OCXO) is supplied at pin MCLK as master clock. TCXO or OCXO should be carefully chosen as required by application. It is recommended that the oscillator is placed close to the STC5420. Frequency of the master oscillator has four options, see description of the register **MCLK Freq Reset** for details.

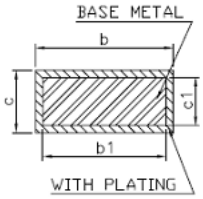
Mechanical Specifications







DETAIL "X"
(20/1)



SECTION A-A

SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.20			47
A1	0.05		0.15	2		6
A2	0.95	1.00	1.05	37	39	41
b	0.17	0.22	0.27	7	9	11
b1	0.17	0.20	0.23	7	8	9
c	0.09		0.20	4		8
c1	0.09		0.16	4		6
D	16.00 BSC			630 BSC		
D1	14.00 BSC			551 BSC		
E	16.00 BSC			630 BSC		
E1	14.00 BSC			551 BSC		
e	0.50 BSC			20 BSC		
L	0.45	0.60	0.75	18	24	30
L1	1.00 REF			39 REF		
R1	0.08			3		
R2	0.08		0.20	3		8
Y			0.075			3
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
s	0.20			8		

NOTES:
1.REFER TO JEDEC MS-026/AED REV. B
2.DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE
MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE
DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED
THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
4.ALL DIMENSIONS IN MILLIMETERS.

Revision History

The following table summarizes significant changes made in each revision. Additions reference current pages.

Revision	Change Description	Pages
0.4	Preliminary initial issue	See particular revision
0.4.1	Minor releases at Preliminary status	
0.5	Minor releases at Preliminary status (Completely revised for new design)	
1.0	First release at final status	All pages
1.1	Add supported frequency of external oscillator	1
	Add G.8262 EEC option1 and option 2	1, 16
	Correct pin number of SRCSW and AD1 to 18 and 82.	7, 8
	Correct registers address of Master_Frame_Align from 0x63-0x64 to 0x40-0x47	10
	Add register EX_SYNC_Edge_Config and Slave_Frame_Align to Table 2	10
	Correct the description of the register 0x7F in Table 2	11
	Add Master Clock Frequency section	12
	Add Clock Output Jitter section	14
	Remove word “reboot”	19, 27, 56, 57
	Correct description of t_{Dd2} in Motorola Bus Read Timing	29
	Correct description of t_{Dd1} in Intel Bus Read Timing	31
	Correct $\overline{CS}$ and RDB to $\overline{WR}$ in the description of Intel Bus Write Timing	32
	Correct description of t_{ALEd} of Multiplex Bus Write Timing	34
	Add more detail description to section Chip Master Clock	17
	Add more detail description of the register MCLK_Freq_Reset	57, 58
1.2	Change mechanical specifications due to assembly change	63
1.3	Correct SPI Bus Timing, Write access	29

2.0	Update Funtional diagram	1
	Remove LVCMOS level for REF11 and REF12	1, 13, 16, 22
	Add register Frame_Mux and Diff_Ref_Polarity	11, 57, 58
	Change register CLK8K_Sel and CLK2K_Sel to Frame8K_Sel and CLK2K_Sel	11, 56
	Change name of register Ref_Freq to Ref_Acceptable_Freq	13, 22, 57
	Add description of frame mux	25, 26,
	Update CLK3~CLK8, CLK8K and CLK2K detail diagram in Figure 6, 7	25, 26
	Rephase Master Slave Configuration	26
	Correct SDI of SPI Bus Timing, Write access	29
	Correct t_{CH} and t_{CL}, LSB to MSB and MSB to LSB in serial bus timing figure	28, 29
	Correct Min value of t_{CH} and t_{CL} to 50ns in serial bus timing table	29
	Correct description of t_{CSHLD} and t_{CSTRI} in serial bus timing table	29
	Update register Ref_Info Interrupt_Event_Sts, PLL_Event_Out, PLL_Event_In, CLK(3~8)_Sel, Synth_Index_Select, Synth_Freq_Value, Synth_Skew_Adj	40, 48, 52, 53, 54, 55, 56
	Update order information	63
	Add section of Specification Modification	64
	Miscellaneous	All pages

For more information, contact:

CONNOR WINFIELD

2111 Comprehensive DR
Aurora, IL. 60505, USA
630-851-4722
630-851-5040 FAX
www.conwin.com