

High Precision TCXO /VCTXCO

CONNOR WINFIELD



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Description:

The Connor-Winfield 5.0x7.0mm Temperature Compensated Crystal Controlled Oscillators and Voltage Controlled Temperature Compensated Crystal Controlled Oscillators are designed for use in applications requiring tight frequency stability in a small package. Through the use of Analog Temperature Compensation, this device is capable of holding sub 1-ppm stabilities over the commercial or the industrial temperature ranges.



Features:

- 3.3V Operation
- CMOS or Clipped Sinewave Output Logic
- Frequency Stabilities Available:
 - Tx5C / Tx6C Series: ± 0.25 ppm
 - Tx5E / Tx6E Series: ± 0.50 ppm
 - Tx5F / Tx6F Series: ± 1.00 ppm
- Temperature Ranges Available:
 - Tx5x Series: 0 to 70°C
 - Tx6x Series: -40 to 85°C
- Low Jitter <1pS RMS
- Tri-State Enable/Disable Function
- Miniature 5x7mm Surface Mount Package
- Tape and Reel Packaging
- RoHS Compliant / Lead Free
- Recommended for new designs

Applications:

- GPS Receivers
- Instrumentation
- Femtocells
- FTTH, FTTC

Standard Frequencies Available *

6.4 MHz 9.72 MHz 10.0 MHz 10.24 MHz 12.5 MHz 19.44 MHz 20.0 MHz 20.48 MHz
12.8 MHz 13.5 MHz 19.2 MHz 25 MHz 27 MHz 38.88 MHz

* Available frequencies from the factory for small quantity orders or quick delivery. Additional frequencies are available.

Ordering Information

T	A	5	C	020.0M
Type: Precision TCXO VCTXCO 5x7mm	Features: A = TCXO, LVCMOS, 3.3Vdc B = TCXO, Clipped Sinewave, 3.3Vdc E = VCTXCO, LVCMOS, 3.3Vdc F = VCTXCO, Clipped Sinewave, 3.3Vdc	Temperature Range: 5 = 0 to 70°C 6 = -40 to 85°C	Frequency Stability: C = ± 0.25 ppm E = ± 0.50 ppm F = ± 1.00 ppm	Output Frequency: Frequency Format -xxx.xM Min.* -xxx.xxxxxM Max.* *Maximum of 6 digits after the decimal point. M=MHz

Example:
TA5C-020.0M = 5x7mm, TCXO, LVCMOS,
3.3Vdc, 0 to 70C, +/-0.25ppm, Output Frequency 20.0MHz

To order an TA5C with an output frequency of:
6.4 MHz = TA5C-006.4M
10 MHz = TA5C-010.0M
38.88 MHz = TA5C-038.88M





Model Specifications

±0.25ppm Model Specifications

Model Number	TA5C	TB5C	TE5C	TF5C
Output Type	LVC MOS	Clipped Sinewave	LVC MOS	Clipped Sinewave
TCXO / VCTCXO	TCXO	TCXO	VCTCXO	VCTCXO
Supply Voltage	3.3Vdc	3.3Vdc	3.3Vdc	3.3Vdc
Frequency Range	6.4 to 40 MHz			
Frequency Stability vs Temperature [$\pm(F_{max}-F_{min})/2F_0$]	±0.25ppm			
Temperature Range	0 to 70°C			
Model Number	TA6C	TB6C	TE6C	TF6C
Output Type	LVC MOS	Clipped Sinewave	LVC MOS	Clipped Sinewave
TCXO / VCTCXO	TCXO	TCXO	VCTCXO	VCTCXO
Supply Voltage	3.3Vdc	3.3Vdc	3.3Vdc	3.3Vdc
Frequency Range	6.4 to 40 MHz			
Frequency Stability vs Temperature [$\pm(F_{max}-F_{min})/2F_0$]	±0.25ppm			
Temperature Range	-40 to 85°C			

±0.50ppm Model Specifications

Model Number	TA5E	TB5E	TE5E	TF5E
Output Type	LVC MOS	Clipped Sinewave	LVC MOS	Clipped Sinewave
TCXO / VCTCXO	TCXO	TCXO	VCTCXO	VCTCXO
Supply Voltage	3.3Vdc	3.3Vdc	3.3Vdc	3.3Vdc
Frequency Range	6.4 to 50 MHz			
Frequency Stability vs Temperature [$\pm(F_{max}-F_{min})/2F_0$]	±0.50ppm			
Temperature Range	0 to 70°C			
Model Number	TA6E	TB6E	TE6E	TF6E
Output Type	LVC MOS	Clipped Sinewave	LVC MOS	Clipped Sinewave
TCXO / VCTCXO	TCXO	TCXO	VCTCXO	VCTCXO
Supply Voltage	3.3Vdc	3.3Vdc	3.3Vdc	3.3Vdc
Frequency Range	6.4 to 50 MHz			
Frequency Stability vs Temperature [$\pm(F_{max}-F_{min})/2F_0$]	±0.50ppm			
Temperature Range	-40 to 85°C			

±1.00ppm Model Specifications

Model Number	TA5F	TB5F	TE5F	TF5F
Output Type	LVC MOS	Clipped Sinewave	LVC MOS	Clipped Sinewave
TCXO / VCTCXO	TCXO	TCXO	VCTCXO	VCTCXO
Supply Voltage	3.3Vdc	3.3Vdc	3.3Vdc	3.3Vdc
Frequency Range	6.4 to 50 MHz			
Frequency Stability vs Temperature [$\pm(F_{max}-F_{min})/2F_0$]	±1.00ppm			
Temperature Range	0 to 70°C			
Model Number	TA6F	TB6F	TE6F	TF6F
Output Type	LVC MOS	Clipped Sinewave	LVC MOS	Clipped Sinewave
TCXO / VCTCXO	TCXO	TCXO	VCTCXO	VCTCXO
Supply Voltage	3.3Vdc	3.3Vdc	3.3Vdc	3.3Vdc
Frequency Range	6.4 to 50 MHz			
Frequency Stability vs Temperature [$\pm(F_{max}-F_{min})/2F_0$]	±1.00ppm			
Temperature Range	-40 to 85°C			

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Absolute Maximum Ratings

Parameter	Minimum	Nominal	Maximum	Units	Notes
Storage Temperature	-55	-	125	°C	
Supply Voltage (Vcc)	-0.6	-	4.6	Vdc	
Input Voltage	-0.5	-	Vcc + 0.6	Vdc	

Operating Specifications

Parameter	Minimum	Nominal	Maximum	Units	Notes
TCXO Frequency Calibration @ 25°C	-1.00	-	1.00	ppm	1
Supply Voltage Variation. (Vcc±5%)	-0.05	-	0.05	ppm	
Load Coefficient, ±5%	-0.05	-	0.05	ppm	
Static Temperature Hysteresis	-0.4	-	0.4	ppm	2
Aging	-1.00	-	1.00	ppm / year	
Frequency shift after reflow soldering	-1.00	-	1.00	ppm	3
Supply Voltage (Vcc)	3.135	3.3	3.465	Vdc	
Supply Current (Icc) LVCMOS:	-	3	6.5	mA	
Clipped Sine:	-	2	3.5	mA	
Jitter:					
Period Jitter	-	3.0	5.0	ps RMS	
Integrated Phase Jitter (12kHz to Fo/2 MHz)	-	0.3	1.0	ps RMS	4
Allan Deviation (1s)	-	1.0E-10	-		
Typical SSB Phase Noise					
For Fo	10.0 MHz	25.0 MHz	50.0 MHz		
@ 10 Hz offset	-98	-90	-73	dBc/Hz	
@ 100 Hz offset	-125	-120	-103	dBc/Hz	
@ 1 KHz offset	-143	-140	-134	dBc/Hz	
@ 10 KHz offset	-151	-151	-151	dBc/Hz	
@ 100 KHz offset	-152	-152	-152	dBc/Hz	
@ 1 MHz offset	-155	-154	-154	dBc/Hz	
Startup Time	-	-	10	ms	

Input Characteristics for Enable / Disable Function (Pin 8)

Parameter	Minimum	Nominal	Maximum	Units	Note
Enable Voltage (High) or open circuit (Vih)	70% Vcc	-	-	Vdc	5
Disable Voltage (Low) Output Tri-stated (Vil)	-	-	30% Vcc	Vdc	

Input Characteristics for Voltage Control (Pin 10)

Parameter	Minimum	Nominal	Maximum	Units	Note
Control Voltage Range (Vcc = 3.3V) (Vc)	0.30	1.65	3.00	Vdc	
Frequency Tuning measured @ 25°C	±10	-	-	ppm	6
Linearity	±5	-	-	%	
Slope		Positive			
Input Impedance	100K	-	-	Ohms	



CMOS Output Characteristics

Parameter	Minimum	Nominal	Maximum	Units	Note
LOAD	-	15	-	pF	7
Voltage (High) (Voh)	90%Vcc	-	-	Vdc	
(Low) (Vol)	-	-	10%Vcc	Vdc	
Current (High) (Ioh)	-	-	-4	mA	
(Low) (Iol)	4	-	-	mA	
Duty Cycle at 50% of Vcc	45	50	55	%	
Rise / Fall Time 10% to 90%	-	4	8	ns	

Clipped Sinewave Output Characteristics

Parameter	Minimum	Nominal	Maximum	Units	Note
Load					8
Output Load Resistance	-	10K	-	Ohms	
Output Load Capacitance	-	10	-	pF	
Output Voltage (≤ 40 MHz)	1.0	1.2	-	V pk-pk	
Output Voltage (>40 MHz)	0.8	1.0	-	V pk-pk	

Package Characteristics

Package	Ceramic Surface Mount Package
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Environmental Characteristics

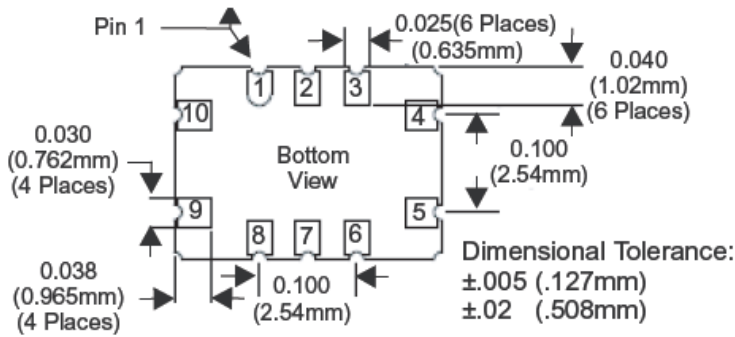
Vibration	Vibration per Mil Std 883E Method 2007.3 Test Condition A
Shock	Mechanical Shock per Mil Std 883E Method 2002.4 Test Condition B
Soldering Process	RoHS compliant lead free. See soldering profile on Page 5
Solderability	Solderability per Mil Std 883E Method 2003

Notes:

- 1) Initial calibration @ 25°C. $\pm 2^\circ\text{C}$, for VCTCXO, control voltage must be set to nominal value. Specifications at time of shipment.
- 2) Frequency change after reciprocal temperature ramped over the operating range. Frequency measured before and after at 25°C.
- 3) Two consecutive solder reflows after 1 hour recovery @ 25°C.
- 4) BW = 12 KHz to 20 MHz.
- 5) Leave Pad 8 unconnected if enable / disable function is not required. When tristated, the output stage is disabled but the oscillator and compensation circuit are still active (current consumption < 1 mA).
- 6) Additional pull ranges are available; please contact the factory for additional information.
- 7) Attention: To achieve the frequency stability specified it is required that the circuit connected to this TCXO output must have the equivalent input capacitance that is specified by the nominal load capacitance.
- 8) Output is AC coupled.

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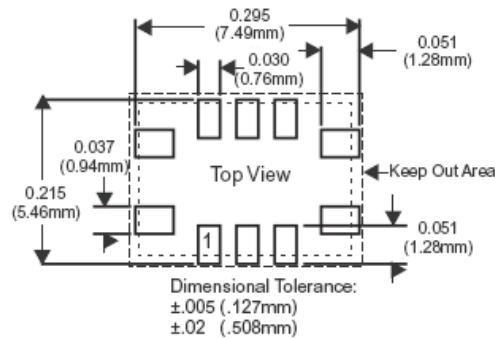
Package Pad Configuration (all models)



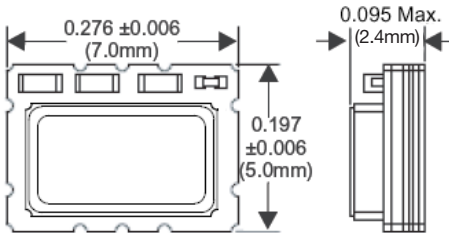
Pad Connections (all models)

1	Do not connect
2	Do not connect
3	Do not connect
4	Ground
5	Output
6	Do not connect
7	Do not connect
8	Tri-state Enable / Disable
9	Supply, Vcc
10	Voltage Control (VCTCXO) N/C (TCXO)

Suggested Pad Layout (all models)



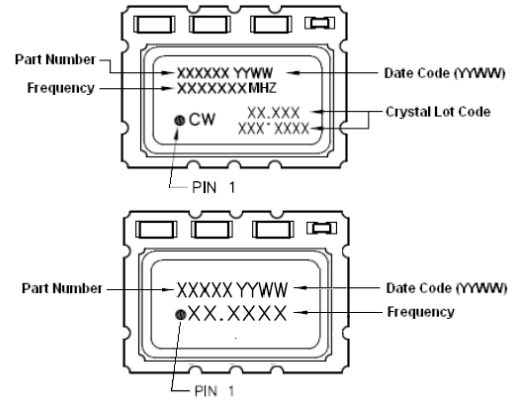
Package Configuration #1



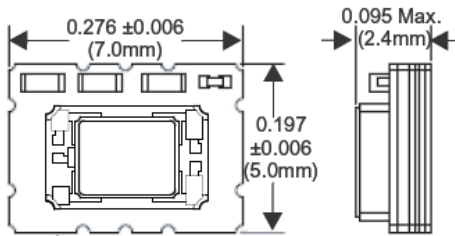
Models

All models except those listed in configurations 2 and 3 below.

Marking Configurations



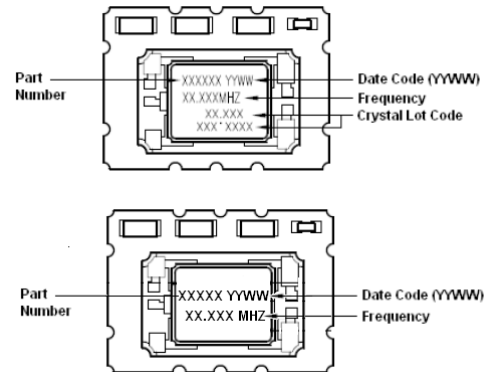
Package Configuration #2



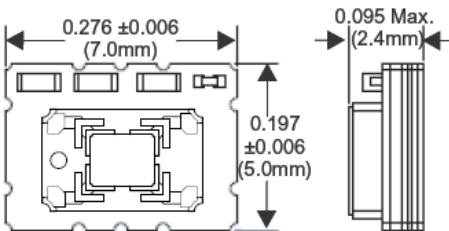
Models

TA6E-040.0M
TA6F-040.0M
TA6F-048.0M
TE6F-050.0M
TF6F-050.0M

Marking Configurations



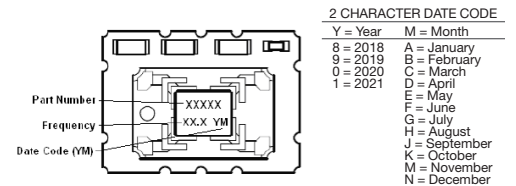
Package Configuration #3



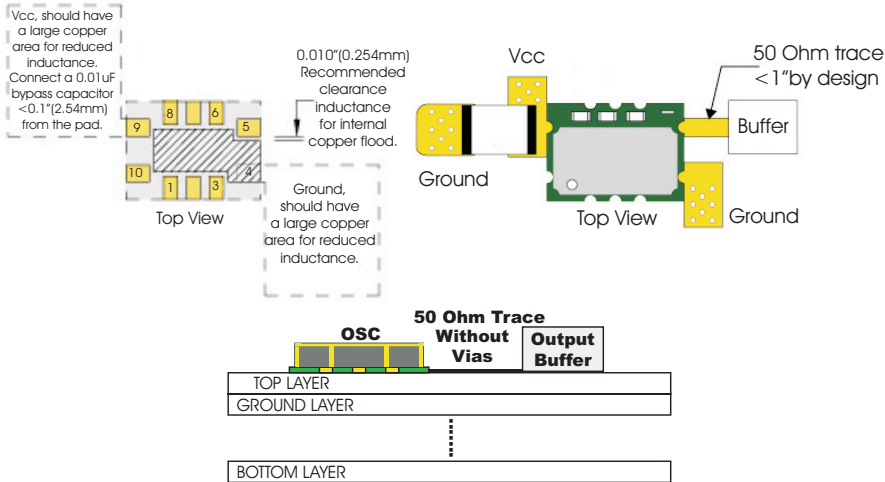
Models

TA6C-040.0M

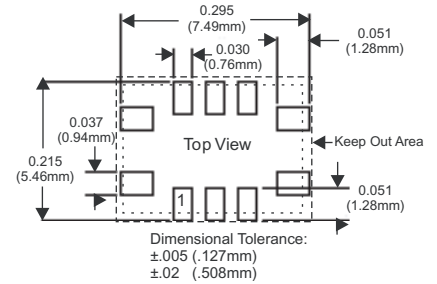
Marking Configurations



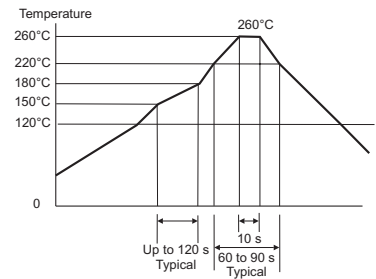
Design Recommendations



Suggested Pad Layout

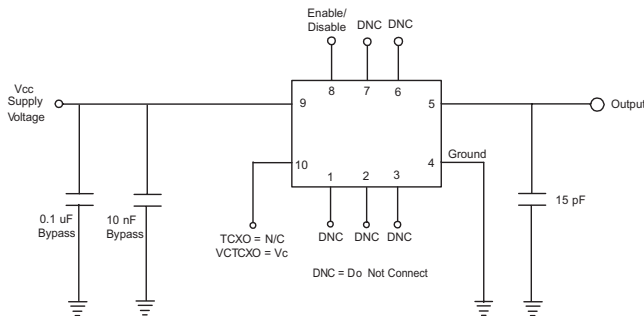


Solder Profile

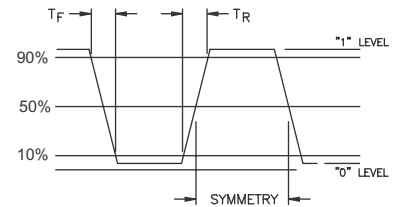


Meets IPC/JEDEC J-STD-020C

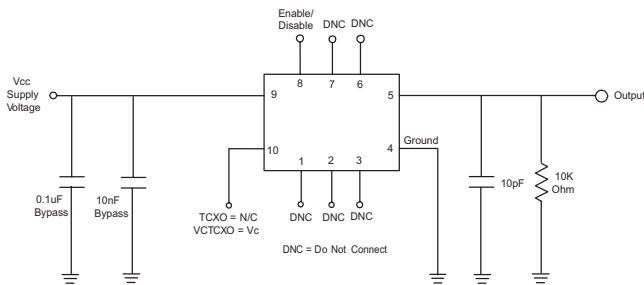
CMOS Test Circuit



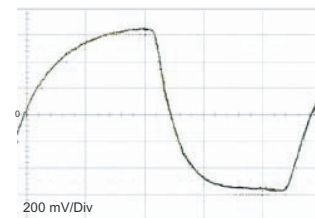
CMOS Output Waveform



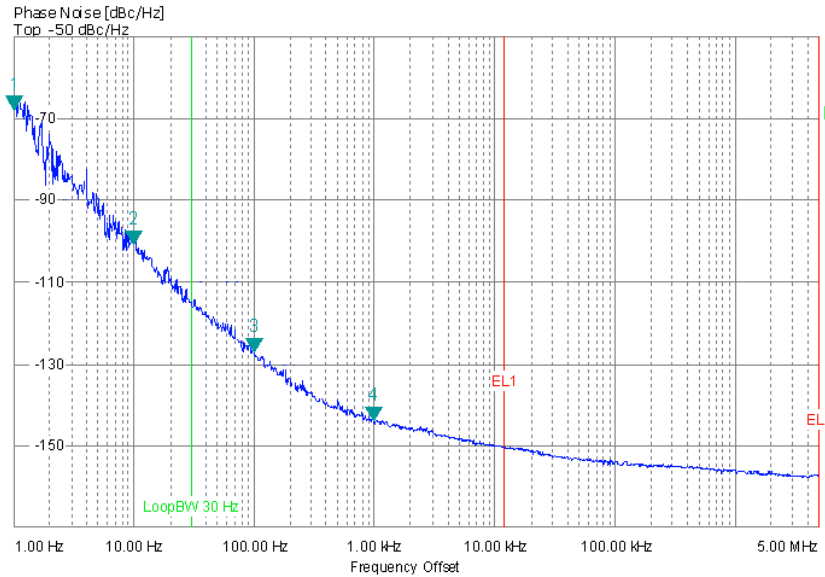
Clipped Sinewave Test Circuit



Clipped Sinewave Output Waveform

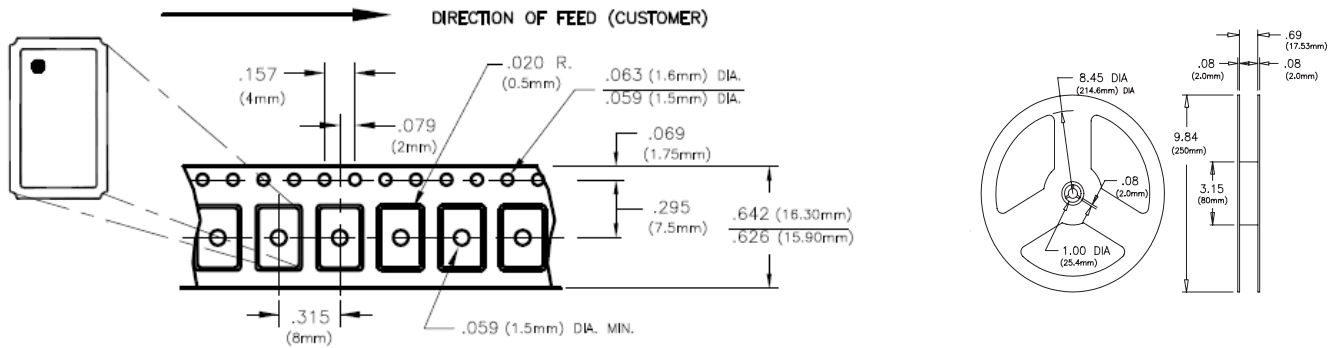


Typical Phase Noise at Fo=10MHz



5x7mm Tape and Reel Information

MEETS EIA-481A AND EIAJ-1009B
700 PCS/REEL MAXIMUM.



Revision History

Revision	Date	Note
11	09/07/18	Updated package drawing height and T&R information, added marking configurations.
12	10/10/18	Updated package drawings
13	02/07/23	Updated Package Configuration #1
14	11/15/23	Updated Voltage Operation

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