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## 5x7mm Precision TCXO Model DV75C

**CONNOR  
WINFIELD**



### Description:

The Connor-Winfield's DV75C is a 5x7mm Surface Mount Temperature Compensated Crystal Controlled Oscillator (TCXO) with LVCMOS output. Through the use of Analog Temperature Compensation the DV75C is capable of holding sub 1-ppm stabilities over the -40 to 85°C temperature range. The DV75C meets STRATUM 3 requirements.



### Features:

- 3.3 Vdc Operation
- LVCMOS Output
- Frequency Stability:  $\pm 0.28$  ppm
- Temperature Range: -40 to 85°C
- Low Jitter <1ps RMS
- 5x7mm Surface Mount Package
- Tape and Reel Packaging
- RoHS Compliant / Pb Free

### Applications:

- IEEE 1588 Applications
- Synchronous Ethernet slave clocks, ITU-T G.8262 EEC options 1 & 2
- Compliant to Stratum 3, GR-1244-CORE, GR-253-CORE & ITU-T-G.812 Type IV
- Wireless Communications
- Small Cells
- Test and Measurement

### Absolute Maximum Ratings

Parameter	Minimum	Nominal	Maximum	Units	Notes
Storage Temperature	-55	-	95	°C	
Supply Voltage (Vcc)	-0.6	-	4.6	Vdc	
Input Voltage	-0.5	-	Vcc+0.6	Vdc	

### Operating Specifications

Parameter	Minimum	Nominal	Maximum	Units	Notes
Nominal Frequencies (Fo) available	10.0, 12.8, 20.0, 25.0 and 40.0			MHz	
Frequency Calibration @ 25 °C	-1.0	-	1.0	ppm	1
Frequency Stability vs. Temperature	-0.28	-	0.28	ppm	2
Holdover Stability (Over 24 Hours)	-0.32	-	0.32	ppm	3
Frequency vs. Load Stability	-0.05	-	0.05	ppm	$\pm 5\%$
Frequency vs. Voltage Stability	-0.05	-	0.05	ppm	$\pm 5\%$
Static Temperature Hysteresis	-	-	0.4	ppm	4
Total Frequency Tolerance:	-4.6	-	4.6	ppm	5
Operating Temperature Range:	-40	-	85	°C	
Supply Voltage (Vcc)	3.135	3.3	3.465	Vdc	$\pm 5\%$
Supply Current (Icc)	-	-	6	mA	
Period Jitter	-	3	5	ps rms	
Integrated Phase Jitter	-	0.5	1.0	ps rms	6
Typical Phase Noise Fo = 10.0 MHz					
SSB Phase Noise at 10Hz offset	-	-103	-	dBc/Hz	
SSB Phase Noise at 100Hz offset	-	-128	-	dBc/Hz	
SSB Phase Noise at 1KHz offset	-	-147	-	dBc/Hz	
SSB Phase Noise at 10KHz offset	-	-157	-	dBc/Hz	
SSB Phase Noise at 100KHz offset	-	-158	-	dBc/Hz	
Start-up Time	-	-	10	ms	

### LVCMOS Output Characteristics

Parameter	Minimum	Nominal	Maximum	Units	Notes
Load	-	15	-	pF	7
Voltage (High) (Voh)	90%Vcc	-	-	Vdc	
(Low) (Vol)	-	-	10%Vcc	Vdc	
Duty Cycle at 50% of Vcc	45	50	55	%	
Rise / Fall Time 10% to 90%	-	-	8	ns	

### Notes:

1. Initial calibration @ 25°C. Specifications at time of shipment after 48 hours of operation.
2. Frequency stability vs. change in temperature.  $[(F_{max} - F_{min}) / (2 \cdot F_0)]$ .
3. Inclusive of frequency stability, supply voltage change ( $\pm 1\%$ ), load change, aging, for 24 hours.
4. Frequency change after reciprocal temperature ramped over the operating range. Frequency measured before and after at 25°C.
5. Inclusive of calibration @ 25°C, frequency vs. change in temperature, change in supply voltage ( $\pm 5\%$ ), load change ( $\pm 5\%$ ), reflow soldering process and 20 years aging, referenced to Fo.
6. BW = 12 KHz to Fo/2 MHz.
7. For best performance it is recommended that the circuit connected to this output should have an equivalent input capacitance of 15pF.



Package Characteristics

Package	Ceramic Surface Mount Package.
Moisture Sensitivity Level	MSL-1.
Pad Termination Material and Plating	0.5-1.0um [20-40 micro-inches] Gold over 1.27um [50micro-inches] min Nickel.

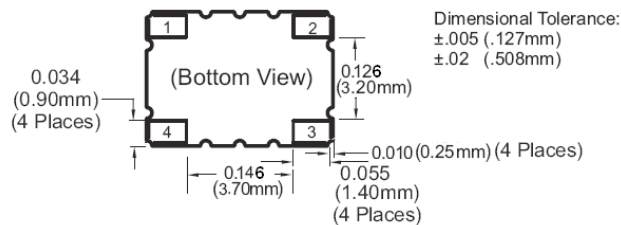
Environmental Characteristics

Vibration:	Vibration per Mil Std 883E Method 2007.3 Test Condition A.
Shock:	Mechanical Shock per Mil Std 883E Method 2002.4 Test Condition B.
Soldering Process:	RoHS compliant lead free. See soldering profile on page 3.
Solderability:	Solderability per Mil Std 883E Method 2003.

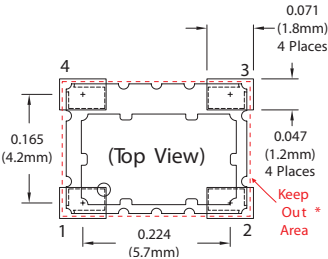
Ordering Information

DV75C-010.0M, DV75C-012.8M, DV75C-020.0M, DV75C-025.0M, DV75C-040.0M

Package Layout (All Configurations)



Suggested Pad Layout

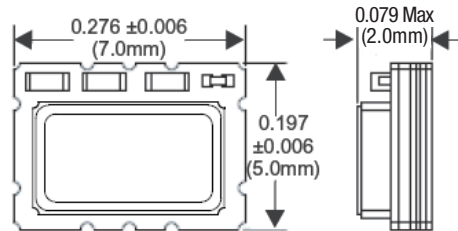


Pad Connections

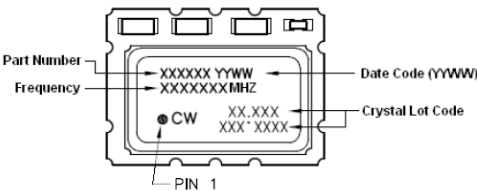
1:	N/C
2:	Ground
3:	Output (Fo)
4:	Supply Voltage (Vcc)

\* Do not route any traces in the keep out area.  
It is recommended the next layer under the keep out area is to be ground plane.

Package Configuration #1



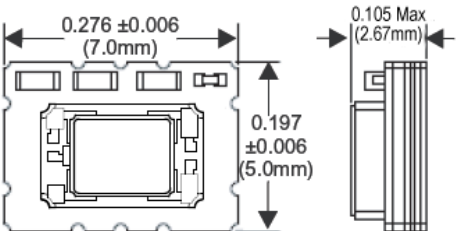
Marking Configuration



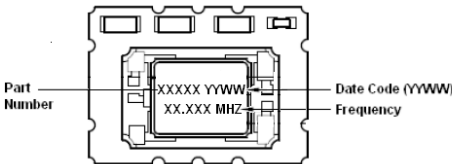
Frequencies

12.8M

Package Configuration #2



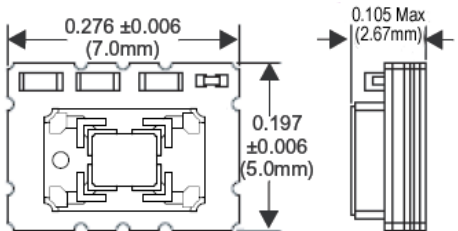
Marking Configuration



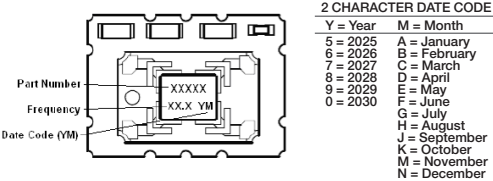
Frequencies

10M  
20M

Package Configuration #3



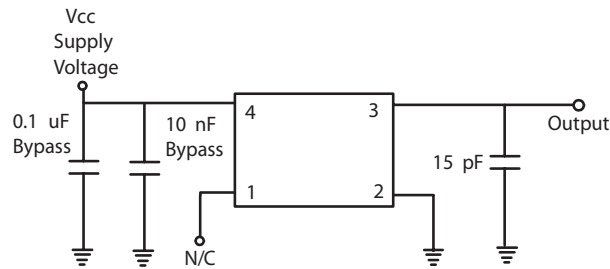
Marking Configuration



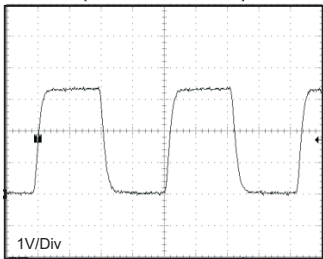
Frequencies

25M  
40M

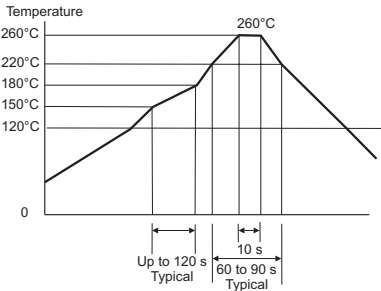
Test Circuit



Output Waveform

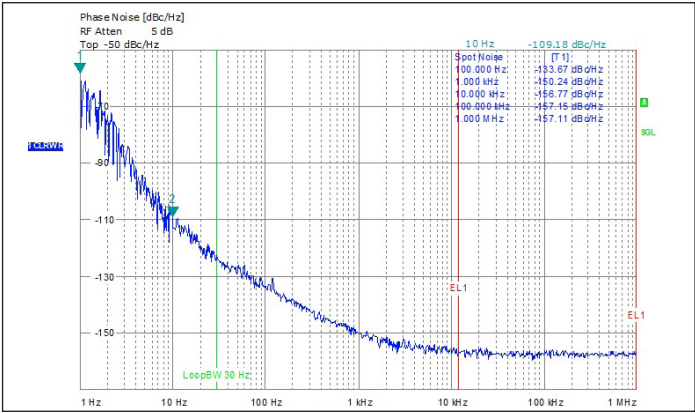


Solder Profile

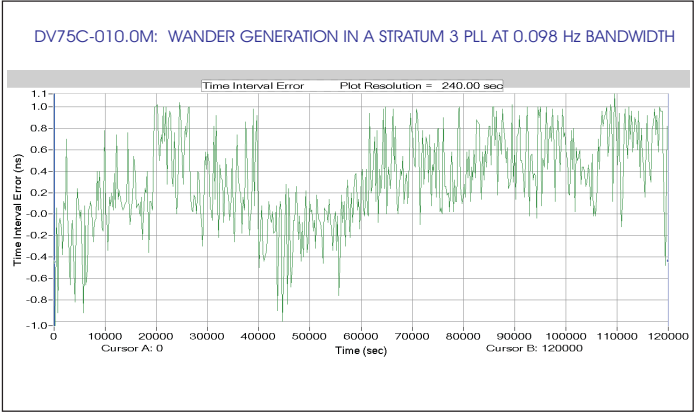


Meets IPC/JEDEC J-STD-020C

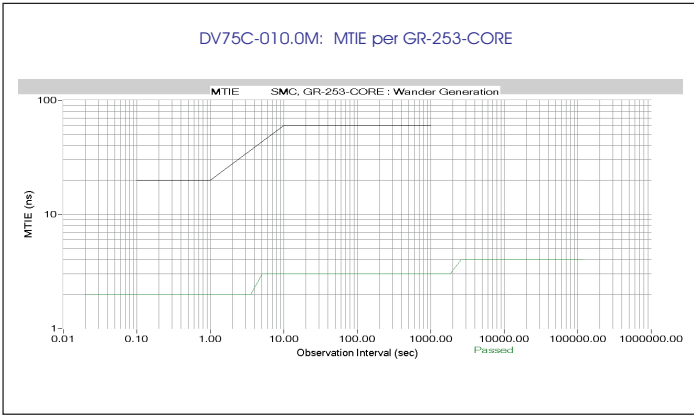
Phase Noise Information  
Typical Phase Noise for DV75C-010.0M



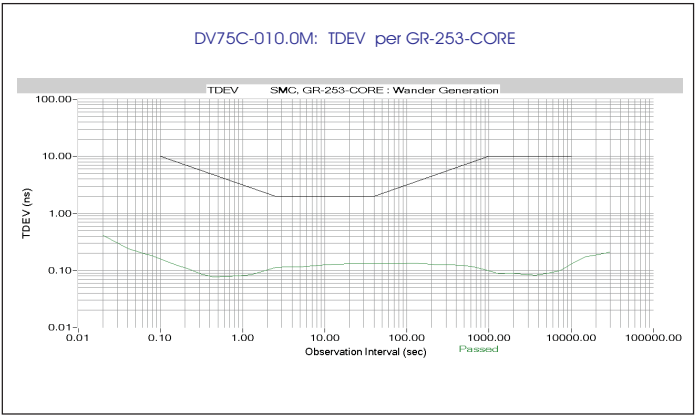
TIE



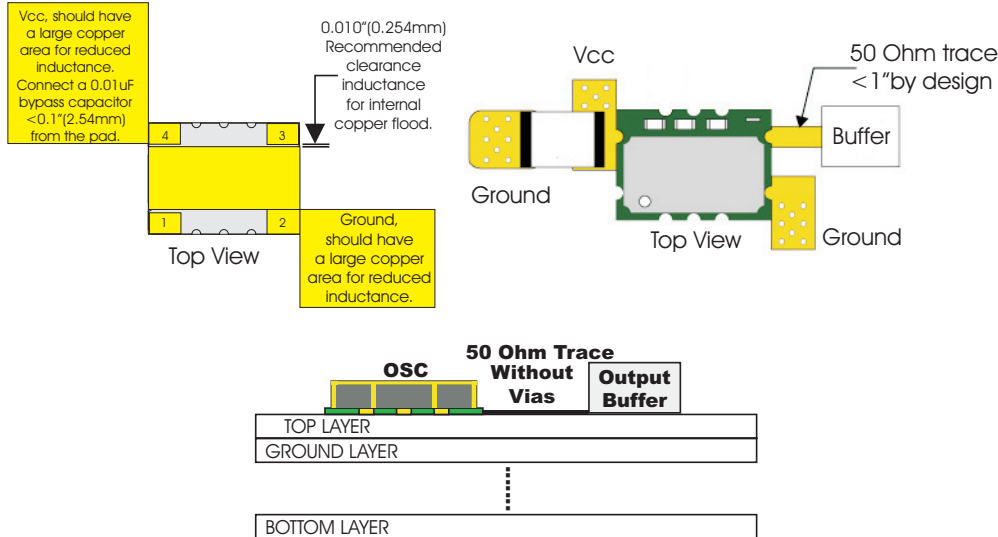
MTIE



TDEV



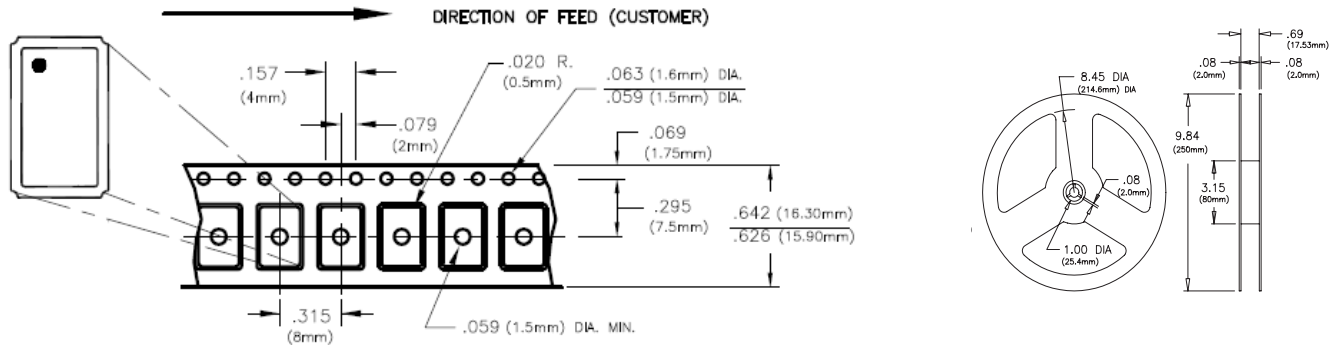
## Design Recommendations



Attention: To achieve optimal frequency stability, and in some cases to meet the specification stated on this data sheet, it is required that the circuit connected to this TCXO output must have the equivalent input capacitance that is specified by the nominal load capacitance. Deviations from the nominal load capacitance will have a graduated effect on the stability of approximately 20 ppb per pF load difference.

## Tape and Reel Dimensions

MEETS EIA-481A AND EIAJ-1009B  
1000 PCS/REEL Max (Package Configuration 1)  
700 PCS/REEL Max (Package Configurations 2 and 3)



## Revision History

Revision	Date	Note
00	01/11/12	Data sheet released
01	11/26/12	Removed tri-state information from features and description.
02	04/15/13	Added "Applications", Phase noise, TIE, MTIE and TDEV plots.
03	12/03/13	Removed TR information from Ordering Information.
04	04/01/15	Add frequencies and update to Phase Noise Plot and Operating Specs
05	11/01/16	Clarify frequencies to which alternate package height applies, and added dimensions to bottom view.
06	11/10/16	Update Static Temperature Hysteresis note and Soldering Process information.
07	11/21/23	Updated Supply Voltage (Vcc)
08	07/24/25	Update phase noise and package dimensions.
09	08/07/25	Update package config 1 height, and Abs Max temperature rating.

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Revision	<b>09</b>
Date	<b>07 Aug 2025</b>