

# 5x7mm Surface Mount Precision TCXO Model T200FA

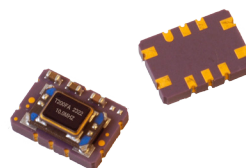
# CONNOR WINFIELD



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## Description:

The Connor-Winfield T200FA is a 5x7mm, 3.3V LVCMOS, Surface Mount, Temperature Compensated Crystal Oscillator (TCXO) designed for applications requiring  $\pm 0.2$  ppm frequency stability over an extended temperature range of -40 to 105°C.



## Features:

### Model: T200FA

- 3.3 Vdc Operation
- Frequency Stability:  $\pm 0.2$  ppm
- Temperature Range: -40 to 105°C
- LVCMOS Output Logic
- Ceramic Surface Mount Package
- Tape and Reel Packaging
- RoHS Compliant / Lead Free

## Absolute Maximum Ratings

Parameter	Minimum	Nominal	Maximum	Units	Notes
Storage Temperature	-55	-	105	°C	
Supply Voltage (Vcc)	-0.5	-	4.6	Vdc	

## Operating Specifications

Parameter	Minimum	Nominal	Maximum	Units	Notes
Output Frequency (Fo)		10		MHz	
Operating Temperature Range	-40	-	105	°C	
Frequency Calibration @ 25 °C	-1.0	-	1.0	ppm	1
Frequency Stability Per STRATUM 3 GR-1244-CORE					
Frequency vs Temperature	-0.2	-	0.2	ppm	2
Holdover Stability	-0.32	-	0.32	ppm	3
Constant Temperature Stability	-40	-	40	ppb	Over 24 Hrs.
Frequency vs. Load Stability	-0.05	-	0.05	ppm	$\pm 5\%$
Frequency vs. Voltage Stability	-0.05	-	0.05	ppm	$\pm 5\%$
Static Temperature Hysteresis	-	-	0.40	ppm	4
Freq. shift after reflow soldering	-1.0	-	1.0	ppm	5
Long Term Stability	-1.0	-	1.0	ppm	6
Aging					
per Life (20 Years)	-3.0	-	3.0	ppm	
per Day	-40	-	40	ppb	
Total Frequency Tolerance	-4.6	-	4.6	ppm	7
Supply Voltage (Vcc)	3.135	3.30	3.465	Vdc	
Supply Current (Icc)	-	2.1	6.0	mA	
Jitter:					
Period Jitter	-	3.0	5.0	ps RMS	
Integrated Phase Jitter	-	0.3	1.0	ps RMS	8
Allan Deviation (1s)	-	1.0E-10	-		
Typical SSB Phase Noise					
@ 10 Hz offset		-112		dBc/Hz	
@ 100 Hz offset		-135		dBc/Hz	
@ 1 KHz offset		-151		dBc/Hz	
@ 10 KHz offset		-158		dBc/Hz	
@ 100 KHz offset		-159		dBc/Hz	
@ 1 MHz offset		-159		dBc/Hz	
Start-Up Time	-	-	10	ms	

## Enable / Disable Input Characteristics

Parameter	Minimum	Nominal	Maximum	Units	Notes
Enable Voltage (High)	70%Vcc		-	Vdc	9
Disable Voltage (Low)	-	-	30%Vcc	Vdc	



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## LVC MOS Output Characteristics

Parameter	Minimum	Nominal	Maximum	Units	Notes
Load (CL)	-	15	-	pF	10
Voltage (High) (Voh)	90%Vcc	-	-	Vdc	
Voltage (Low) (Vol)	-	-	10%Vcc	Vdc	
Duty Cycle at 50% of Vcc	45	50	55	%	
Rise / Fall Time 10% to 90%	-	4	8	ns	

### Notes:

1. Initial calibration @ 25°C. ±2°C.
2. Frequency stability vs. change in temperature.  $[\pm(F_{max}-F_{min})/(2 \cdot F_0)]$ .
3. Inclusive of frequency stability, supply voltage change (±1%), aging, for 24 hours. Per STRATUM 3 GR-1244-CORE.
4. Frequency change after reciprocal temperature ramped over the operating range. Frequency measured before and after at 25°C.
5. Two consecutive solder reflows after 1 hour recovery @ 25°C.
6. Frequency drift over 1 year @ 25°C.
7. Inclusive of calibration @ 25°C, frequency vs. change in temperature, change in supply voltage (±5%), load change (±5%), reflow soldering process and 20 years aging.
8. BW = 12 KHz to 10 MHz
9. Leave Pad 8 on the T Series unconnected if enable / disable function is not required. When tri-stated, the output stage is disabled but the oscillator and compensation circuit are still active (current consumption < 1 mA).
10. Attention: To achieve optimal frequency stability, and in some cases to meet the specification stated on this data sheet, it is required that the circuit connected to this TCXO output must have the equivalent input capacitance that is specified by the nominal load capacitance. Deviations from the nominal load capacitance will have a graduated effect on the stability of approximately 20 ppb per pF load difference.

## Package Characteristics

Package	Hermetically sealed ceramic package and metal cover
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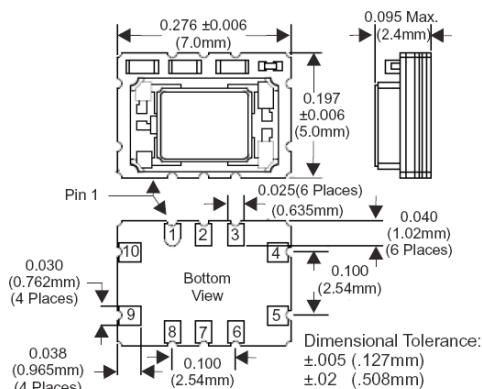
## Environmental Characteristics

Vibration:	Vibration per Mil Std 883E Method 2007.3 Test Condition A
Shock:	Mechanical Shock per Mil Std 883E Method 2002.4 Test Condition B.
Soldering Process:	RoHS compliant lead free. See soldering profile on page 3.

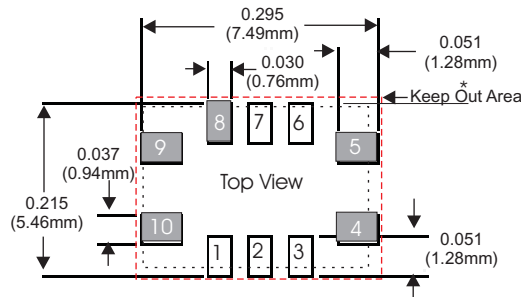
## Ordering Information

T200FA-010.0M

### Package Layout



### Suggested Pad Layout

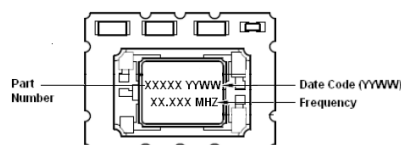


\* Do not route any traces in the keep out area. It is recommended the next layer under the keep out area is to be ground plane.

### Pad Connections

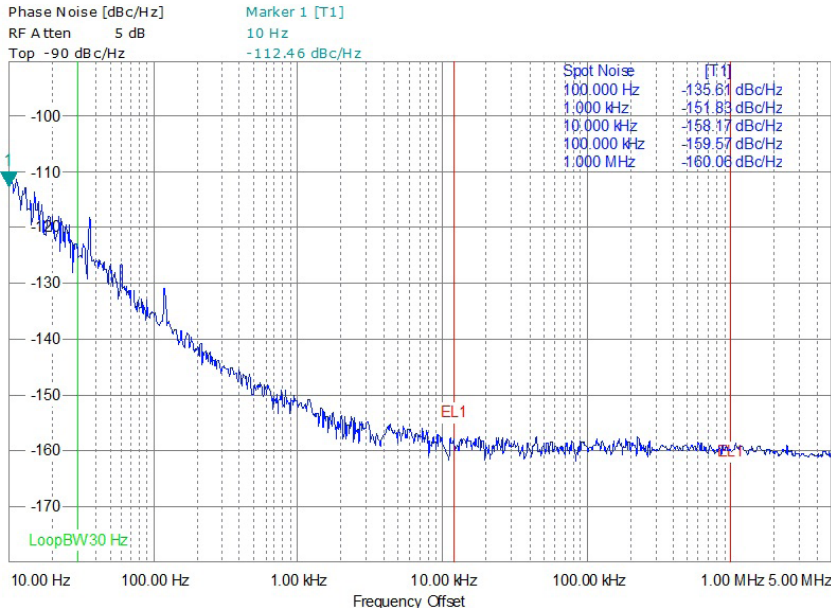
- |     |                    |
|-----|--------------------|
| 1:  | Do Not Connect     |
| 2:  | Do Not Connect     |
| 3:  | Do Not Connect     |
| 4:  | Ground             |
| 5:  | Output             |
| 6:  | Do Not Connect     |
| 7:  | Do Not Connect     |
| 8:  | Enable / Disable   |
| 9:  | Supply Voltage Vcc |
| 10: | N/C                |

## Marking Information

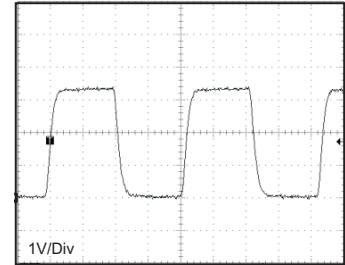


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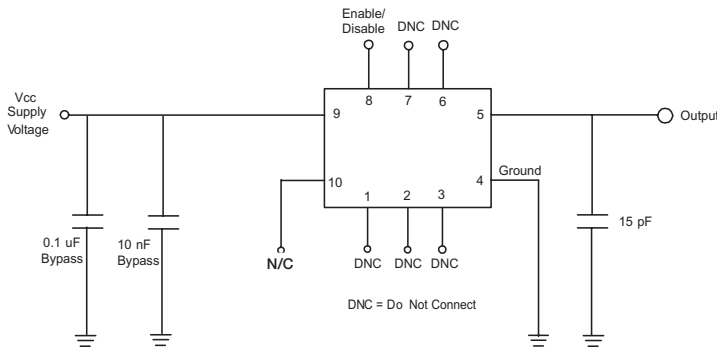
## Phase Noise Plot



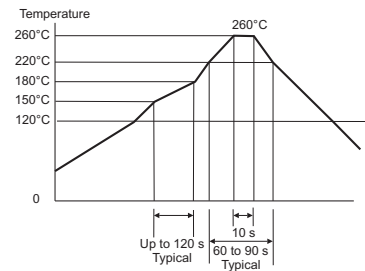
## Output Waveform



## Test Circuit



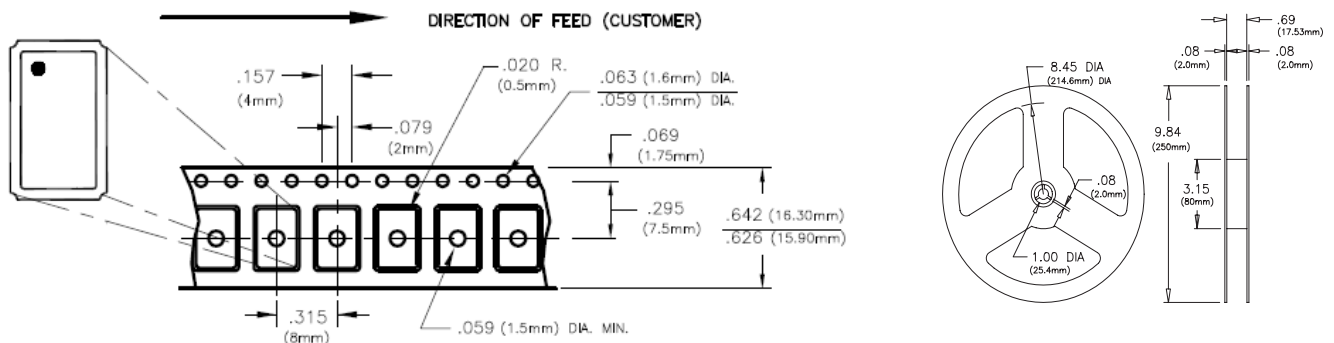
## Solder Profile



Meets IPC/JEDEC J-STD-020C

## Tape and Reel Information

MEETS EIA-481A AND EIAJ-1009B 700 PCS/REEL MAXIMUM.



## Revision History

Revision	Date	Changes
00	05/25/23	Data sheet released
01	05/30/23	Updated photo
02	06/14/23	Updated photo

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