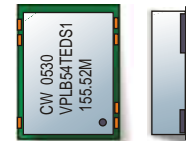


CRYSTAL CONTROLLED OSCILLATORS

3.3V SURFACE MOUNT SELECTABLE OUTPUT VCXO OSCILLATOR



VPLB54TEDS1, VPLB54TEDS2,
VPLB54TEDS3, VPLB54TEDS4

ABSOLUTE MAXIMUM RATINGS

TABLE 1.0

PARAMETER	UNITS	MINIMUM	NOMINAL	MAXIMUM	UNITS	NOTE
Storage Temperature		-40	-	85	°C	
Supply Voltage	(Vcc)	-0.5	-	7.0	Vdc	
Input Voltage		-0.5	-	7.0	Vdc	

MODEL SPECIFICATIONS:

TABLE 2.0

MODEL	PARAMETER	UNITS	MINIMUM	NOMINAL	MAXIMUM	UNITS	NOTE
MODEL VPLB54TEDS1	Center Frequency: Output Select "0"	(Fo)	-	155.5200	-	MHz	
	Center Frequency: Output Select "1"	(Fo)	-	166.6286	-	MHz	
MODEL VPLB54TEDS2	Center Frequency: Output Select "0"	(Fo)	-	156.2500	-	MHz	
	Center Frequency: Output Select "1"	(Fo)	-	167.4107	-	MHz	
MODEL VPLB54TEDS3	Center Frequency: Output Select "0"	(Fo)	-	138.8125	-	MHz	
	Center Frequency: Output Select "1"	(Fo)	-	142.2991	-	MHz	
MODEL VPLB54TEDS4	Center Frequency: Output Select "0"	(Fo)	-	155.5200	-	MHz	
	Center Frequency: Output Select "1"	(Fo)	-	167.3316	-	MHz	

OPERATING SPECIFICATIONS

TABLE 3.0

PARAMETER	UNITS	MINIMUM	NOMINAL	MAXIMUM	UNITS	NOTE
Total Frequency Tolerance		-20	-	20	ppm	1
Operating Temperature Range		0	-	70	°C	
Supply Voltage	(Vcc)	3.135	3.3	3.465	Vdc	
Supply Current	(Icc)	-	-	100	mA	
Jitter (BW=10Hz to 20MHz)		-	-	5	ps rms	
Jitter (BW=12kHz to 80MHz)		-	-	1	ps rms	
SSB Phase Noise at 100Hz offset		-	-60	-	dBc/Hz	
SSB Phase Noise at 1KHz offset		-	-90	-	dBc/Hz	
SSB Phase Noise at 10KHz offset		-	-130	-	dBc/Hz	
SSB Phase Noise at 100KHz offset		-	-140	-	dBc/Hz	

INPUT CHARACTERISTICS

TABLE 4.0

PARAMETER	UNITS	MINIMUM	NOMINAL	MAXIMUM	UNITS	NOTE
Control Voltage Range	(Vc)	0.3	1.65	3.0	Vdc	
Absolute Pull Range (APR)		+/-50	-	-	ppm	2
Monotonic Linearity		-10	-	10	%	
Input Impedance		-	50K	-	Ohm	
Modulation Bandwidth (3dB)		10	-	-	KHz	
Enable Input Voltage (Low)	(Vil)	-	-	1.68	Vdc	3
Disable Input Voltage (High)	(Vih)	2.275	-	-	Vdc	3
Output "0" Select Voltage (Low) (FS)	"0"	-	-	≤30% Vcc	Vdc	
Output "1" Select Voltage (High) (FS)	"1"	≥70% Vcc	-	-	Vdc	

LV PECL OUTPUT CHARACTERISTICS

TABLE 5.0

PARAMETER	UNITS	MINIMUM	NOMINAL	MAXIMUM	UNITS	NOTE
LOAD		-	-	50	Ohms	4
Voltage (High)	(Voh)	2.275	-	-	Vdc	
Voltage (Low)	(Vol)	-	-	1.68	Vdc	
Duty Cycle at 50% Level		45	50	55	%	

PACKAGE CHARACTERISTICS

TABLE 6.0

Package	Non-hermetic package consisting of an FR4 substrate with grounded metal cover.
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PROCESS RECOMMENDATIONS

TABLE 7.0

Solder Reflow	The component solder used internal to this device has a melting point of 221°C. The peak temperature inside the device should be less than or equal to 220°C for a maximum of 10 seconds
Wash	Ultrasonic cleaning is not recommended.

DESCRIPTION

The Connor-Winfield VPLB54TEDS1, VPLB54TEDS2, VPLB54TEDS3 and VPLB54TEDS4 are 3.3V Voltage Controlled Crystal Oscillators (VCXO) with selectable output frequencies and LVPECL Differential outputs. The VPLB54TEDS* series are designed for use with PLL systems in SDH/SONET systems requiring low jitter and tight stability. No uses of multiplication schemes are used in this oscillator design.

FEATURES

SELECTABLE OUTPUT FREQUENCY:

VPLB54TEDS1 - 155.52MHz or 166.6286MHz
VPLB54TEDS2 - 156.25MHz or 167.4107MHz
VPLB54TEDS3 - 138.8125MHz or 142.2991MHz
VPLB54TEDS4 - 155.52MHz or 167.3316MHz

LOW PROFILE, SURFACE MOUNT PACKAGE
3.3V SUPPLY VOLTAGE
LOW JITTER <1ps RMS
FREQUENCY TOLERANCE: ±20ppm
TEMPERATURE RANGE: 0 TO 70°C
DIFFERENTIAL LVPECL OUTPUTS
ENABLE/DISABLE FUNCTION
TAPE AND REEL PACKAGING

ORDERING INFORMATION

VPLB54TEDS1 - 155.52MHz

VCXO
SERIES

CENTER
FREQUENCY

Specifications subject to change without notice.

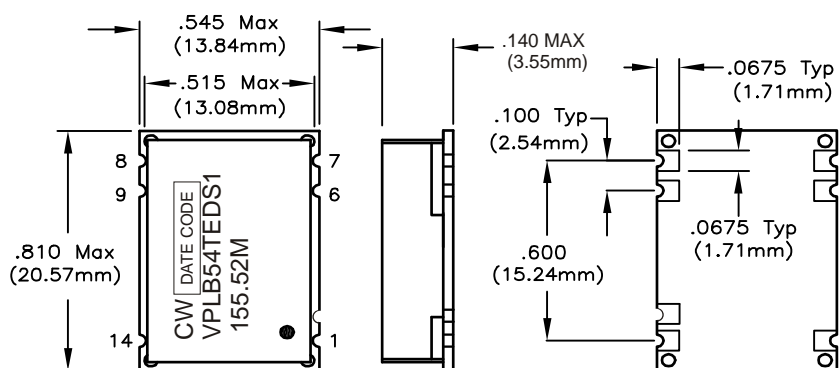
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CRYSTAL CONTROLLED OSCILLATORS

Notes

- 1.0 Inclusive of calibration @ 25°C, frequency stability vs. temperature, supply and load variations, shock, vibration and aging for ten years. Control voltage (Vc) = 1.65 Vdc.
- 2.0 Absolute pull range (APR) is the minimum guaranteed pull range of the VCXO under all conditions over lifetime operation. The APR is referenced to Fo.
- 3.0 Outputs are at high impedance when disabled. Output is enabled with no connection on enable / disable pad 6.
- 4.0 50-ohm termination into Vcc-2V or Thevein equivalent.

Package Layout and Dimensions



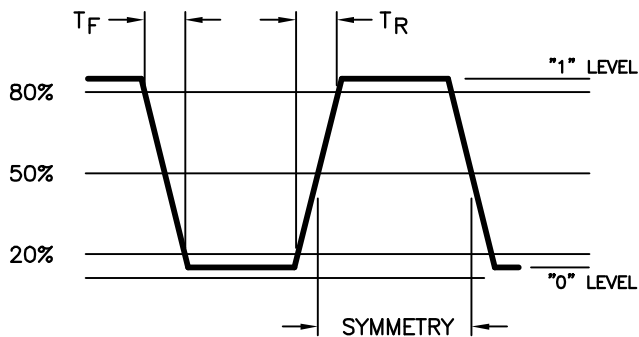
Pin Connections

TABLE 8.0

Pad	Function
1	Control Voltage (Vc)
2	Frequency Select (FS)
6	Enable / Disable
7	Ground (Case)
8	Output Q
9	Comp Output Q
14	Supply Voltage (Vcc)

Dimensional Tolerance:
±.005 (.127mm)

Output Waveform

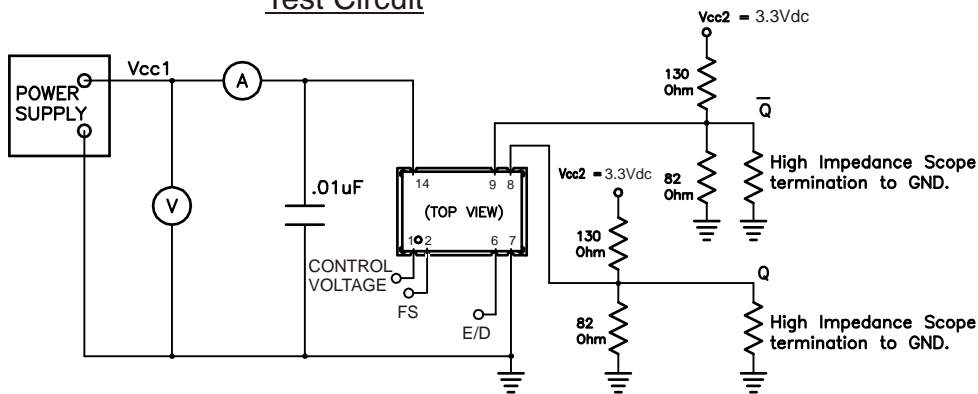


Frequency Select Table

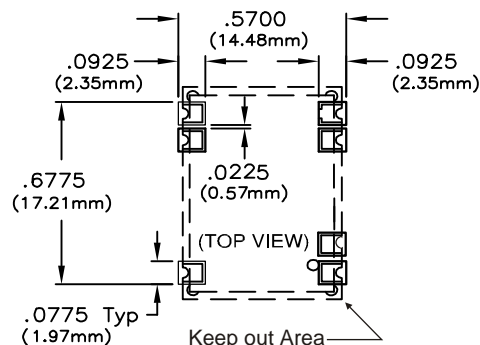
TABLE 9

Model Number	Frequency Select Logic	Output Frequency
VPLB54TEDS1	"0" (Default)	155.5200 MHz
VPLB54TEDS1	"1"	166.6286 MHz
VPLB54TEDS2	"0" (Default)	156.2500 MHz
VPLB54TEDS2	"1"	167.4107 MHz
VPLB54TEDS3	"0" (Default)	138.8125 MHz
VPLB54TEDS3	"1"	142.2991 MHz
VPLB54TEDS4	"0" (Default)	155.5200 MHz
VPLB54TEDS4	"1"	167.3316 MHz

Test Circuit



Suggested Pad Layout



Specifications subject to change without notice.