

High Frequency LVPECL VCXO Model VL7x4 Series

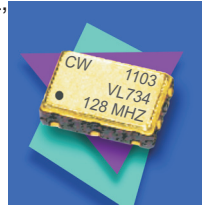
CONNOR WINFIELD



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Description:

The Connor-Winfield VL7x4 series are 5x7mm, 3.3 Vdc LVPECL, Surface Mount, Voltage Controlled Crystal Oscillator (VCXO) designed for phase lock loop applications requiring low jitter and tight frequency stability. The VL7x4 series uses multiplication to achieve the final output frequency. The RoHS compliant surface mount package is designed for high-density mounting and is optimum for mass production.



Features:

3.3V Operation
Absolute Pull Range: ± 100 ppm
Temperature Range Available:
0 to 70°C, -40 to 85°C, 0 to 85°C or
-20 to 70°C
Tri-State Enable/Disable Pad 2
Low Jitter: <1ps RMS
Differential LVPECL Outputs
5x7mm SMT Package
Tape and Reel Packaging
RoHS Compliant / Lead Free

Absolute Maximum Ratings

Parameter	Minimum	Nominal	Maximum	Units	Notes
Storage Temperature	-55	-	125	°C	
Supply Voltage (Vcc)	-0.5	-	4.6	Vdc	
Control Voltage (Vc)	-0.5	-	Vcc + 0.5	Vdc	

Operating Specifications

Parameter	Minimum	Nominal	Maximum	Units	Notes
Center Frequency: (Fo)	65	-	800	MHz	
Operating Temp Range: (See ordering information.)					
Model VL714	0	-	70	°C	
Model VL724	-40	-	85	°C	
Model VL734	0	-	85	°C	
Model VL744	-20	-	70	°C	
Supply Voltage: (Vcc)	3.135	3.3	3.465	Vdc	
Supply Current : (Icc)	-	70	80	mA	
Jitter:					
Period Jitter	-	4	7	ps RMS	
Integrated Phase Jitter	-	0.65	1.0	ps RMS	1
Typical SSB Phase Noise Fo = 128 MHz					
@ 100 Hz offset	-	-80	-	dBc/Hz	
@ 1 KHz offset	-	-105	-	dBc/Hz	
@ 10 KHz offset	-	-120	-	dBc/Hz	
@ 100 KHz offset	-	-125	-	dBc/Hz	
@ 1 MHz offset	-	-135	-	dBc/Hz	
Start-Up Time	-	-	10	ms	

Input Characteristics

Parameter	Minimum	Nominal	Maximum	Units	Notes
Control Voltage Range (Vc)	0.3	1.65	3.0	Vdc	
Pull Slope @ Vc=1.65V	-	120	-	ppm/V	
Absolute Pull Range (APR)	± 100	-	-	ppm	2
Maximum Pull Range @ 25 °C	-	-	± 225	ppm	
Monotonic Linearity	-10	-	10	%	
Input Impedance	2M	-	-	Ohm	
Modulation Bandwidth (3dB)	18	-	-	KHz	
Enable Input Voltage (Low) (Vil)	-	-	0.3Vcc	V	3
Disable Input Voltage (High) (Vih)	0.7Vcc	-	-	V	

LVPECL Output Characteristics

Parameter	Minimum	Nominal	Maximum	Units	Notes
Load	-	50	-	Ohm	4
Voltage (High) Voh	2.275	-	-	V	
(Low) Vol	-	-	1.68	V	
Duty Cycle at 50% Level	45	50	55	%	
Rise / Fall Time: 20% to 80%	-	0.3	0.5	ns	

Package Characteristics

Package Hermetically sealed ceramic surface mount package with case ground metal cover



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- Notes:
- BW= 12 KHz to 20 MHz.
 - Absolute Pull Range (APR) is the minimum guaranteed pull range of the VCXO under all conditions over lifetime operation including calibration @ 25°C, frequency stability vs. the change in temperature, frequency vs. change in supply voltage, frequency vs. change in load, shock and vibration and 10 years aging. The APR is referenced to (Fo). Positive transfer function.
 - Oscillator output is enabled with no connection on pad 2. When the oscillator is disabled the differential outputs are at a high impedance state.
 - Output terminated into 50 ohms into Vcc - 2.0 Vdc or Thevenin equivalent.

Ordering Information

VL7	3	4	128.0M
Type: LVPECL VCXO 5x7 mm Package	Temperature Range 1 = 0 to 70°C 2 = -40 to 85°C 3 = 0 to 85°C 4 = -20 to 70°C	APR and Supply Voltage 4 = ±100 ppm APR Vcc = 3.3 Vdc Enabled = Low ("0")	Output Frequency - Frequency Format -xxx.xM Min. * -xxx.xxxxxM Max. * * Amount of numbers after the decimal point. M = MHz

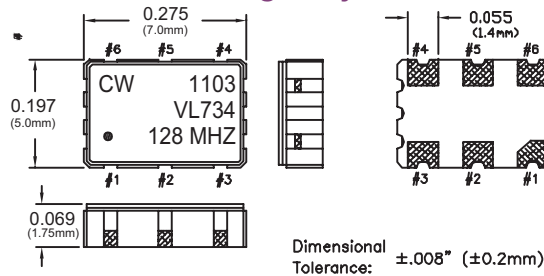
Example Part Number:

VL734-128.0M = 5x7mm, LVPECL, VCXO, 3.3 Vdc, 0 to 85°C, ±100 ppm APR, Output Frequency 128 MHz, Enabled Low ("0").

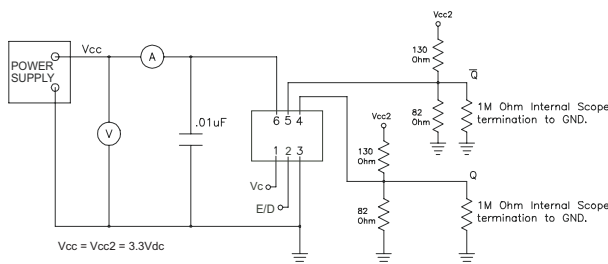
Environmental Characteristics

Vibration:	Vibration per Mil Std 883E Method 2007.3 Test Condition A.
Shock:	Mechanical Shock per Mil Std 883E Method 2002.4 Test Condition B.
Soldering Process:	RoHS compliant lead free. See soldering profile on page 2.

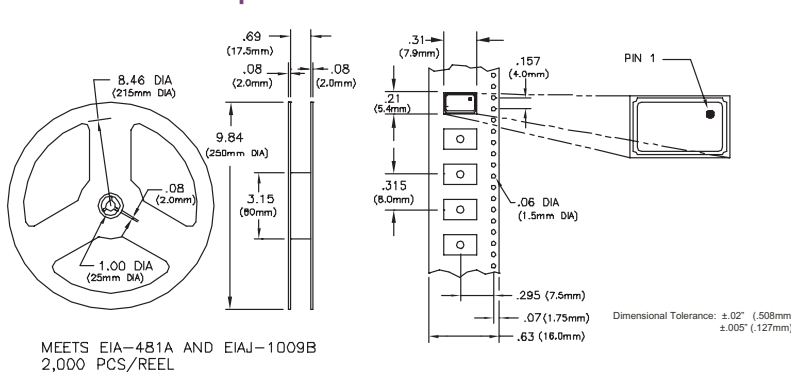
Package Layout



Test Circuit



Tape and Reel Dimensions



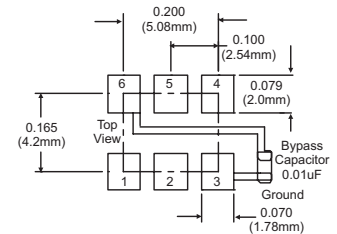
Pad Connections

- Control Voltage (Vc)
- Enable / Disable
- Ground
- Output Q
- Output \bar{Q}
- Supply Voltage (Vcc)

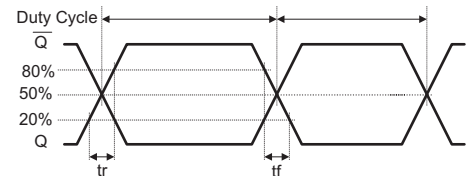
Enable / Disable Function

Function:	Outputs
Low or Open	Enabled
High	Disabled (High Impedance)

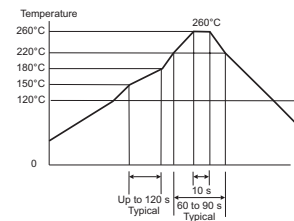
Suggested Pad Layout



Output Waveform



Solder Profile



Meets IPC/JEDEC J-STD-020C

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