CONNOR WINFIELD

Application Note 101

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Selecting Synchronous Timing Modules

Consider an off-the-shelf module that best fits the requirements of the telecommunications design

Introduction

Synchronization is one of the fundamental building blocks of network system design, and al-though this task may appear simple, designing or choosing the appropriate device is not a trivial task. Therefore design engineers should consider an off-the-shelf timing module for their designs (*see Fig.1*), especially if synchronization is new to them or if their resources are limited and they need to concentrate on features that will differentiate their system from the competition.

Standards

Before launching into the design, the engineer must set goals based on telecom network element (NE) synchronization standards, both domestic and international. The main specifications for NE installations are Telcordia's GR-378-CORE, a generic look at synchronization; GR-1244-CORE, a T1 based spec; GR-253-CORE, for SONET covering frequencies that are in multiples of 51.84 MHz (OC1); and ANSI's ANSI-T1-101, that is evolving through regular T1/X1 meetings. ITU-T-G812, ITU-T-G813, and EN 300 462-5-1 cover the international standards.

Once designers have become familiar with the standards that apply to their system, the design can still be a daunting task for those that have little experience with telecom synchronization. As an alternative to designing from scratch, designers can choose off-the-shelf modules that have been pre-audited against the aforementioned standards.

However, there are a variety of types and issues to consider. A designer must choose a synchronous timing module (STM) based on stratum level, filtering characteristics, frequency, options, and lastly, power requirements and packaging. Finally, the designer must select a vendor.

Overview

An STM contains a phase-locked loop (PLL) for reference locking and a control system for maneuvering through the different modes of operation and reporting various conditions. Their specifications vary, depending on where they are in the NE.

Synchronization in an NE begins with two redundant Timing Cards (*see Fig. 2*). The timing cards receive and lock to a stratum 1 reference called Building Integrated Timing Supply (BITS) or to a selected recovered line clock.

The timing cards generate a syn-chronous frequency on the backplane of the NE for the line cards to receive. To complete the timing distribution through the NE, the line cards must also synchronize their rates to the backplane clock.

STMs are broadly classified according to stratum level. Telecom network synchronization follows a hierarchical order from the top down beginning with stratum 1 and ending with stratum 4 (*see table*). All other stratum levels are required to be traceable back to the stratum 1 level through this synchronization hierarchy.

Stratum 1 sources or Primary Reference Sources (PRSs), typically come as GPS based T1 BITS references that reside outside the NE. PRSs also come in the form of stratum 2, but this is more of a legacy requirement. The timing requirement inside the NE is typically that of stratum 3 or stratum 3E.

The cost and performance differences between the stratum 3 and stratum 3E dictate careful planning and consideration. The choice to use either is often made with an assumption that "more-is-better," rather than out of concern for where the NE is within the network, which is more important. SONET minimum clock and stratum 4 or 4E levels are also used within the NE timing cards or line cards, as needs and applications dictate.

Jitter and wander

Jitter and wander are two of the most important considerations for choosing an STM. Jitter is defined as zero crossing noise above 10 Hz, and wander is noise below 10 Hz. Jitter filtering is more important if the reference inputs are from recovered clocks and less important if the reference inputs are from timing cards that already have filtered the clocks.

Typically as you go further downstream, the filtering requirements (bandwidths) become wider. These requirements will vary depending on whether the NE is located in the core, edge, or access part of the network, and whether the module is for the central timing card or the line card.

Loop bandwidth also governs the response time of a system and the extent to which it will filter noise. Jitter filtering requires PLL bandwidths less than 10 Hz. GR-1244 recommends a 3 Hz maximum and GR-253 recommends 0.1 Hz to meet the SONET specifications. The stratum 3E has a loop bandwidth of 0.001 Hz. In the latter two, wander is filtered as well as jitter.

A PLL-based STM has various modes of operation–the primary being locked operation. For the PLL to acquire lock, the reference must be within the pull-in (or tracking) range. For the PLL to remain locked, the reference input must be within both the pull-in and hold-in ranges.

Stratum 3 timing card requirements set the pull-in range to 4.6 ppm minimum. For SONET components, these specifications may go as high as 20 ppm. Line card modules typically need to track 20-ppm references. To guarantee these ranges for 20 years, crystal oscillator PLLs need to account for aging, temperature and other long-term stability perturbations.

For this reason, off-the-shelf synchronous modules will seem, at first, to track much larger ranges. The designer should follow the vendor's datasheet for the pull-in range and not the apparent tracking range of the module on the test bench.

While the module is locked, the phase performance is qualified in terms of maximum time interval error (MTIE) and time deviation (TDEV), both of which are derived from the time interval error (TIE). TIE is essentially a measure of phase deviation over time. MTIE is a plot of the maximum TIE over different observation times and is a measure of wander.

A measure of the stability of a timing module is TDEV, which is derived from Alan Variance. TDEV shows how stable a module is over short-and-long observation times.

Another parameter dependent on system bandwidth is speed at which a module responds to phase transients. Slower response times are generally preferred.

Ideally, the transient response time should be within the limits of the stratum level with less than 0.2 dB peaking. Narrower loop bandwidths improve the module's capability to filter wander and this performance is evident by its wander transfer performance.

Additionally, one must determine the frequency requirements of the system. The backplane frequency can range from 8 kHz to as high as the design can tolerate. Usually 8 kHz, 19.44 MHz. or 77.76 MHz are frequencies commonly accepted as inputs by the framers and line interface units on the line cards.

Jitter needs to be very low since these frequencies are typically multiplied as high as OC-192. A SONET bandwidth of interest is 12 kHz to 20 MHz with jitter requirements usually less than 1 ps rms.

Jitter performance within specific bandwidths can be derived from phase noise plots and calculated for the frequencies of interest. Scrutiny of the telecom chips' specifications will reveal the jitter tolerance of the input clock required to meet system specifications. It is nearly impossible to achieve these low jitter specifications without a fundamental crystal oscillator generating the output. To meet stringent specifications, some ICs require a crystal oscillator PLL to follow them to lower the jitter.

There must at least be two references for redundancy on the timing card. Common reference input frequencies are 8 kHz, T1, E1 and 19.44 MHz.

Holdover and freerun

In addition to locked operation, two other modes of operation to consider are Holdover and Freerun. Holdover mode is an operating condition during which the output frequency is unlocked but it is historically related to a past locked value.

Holdover specifications vary depending on the operating stratum level. Holdover for stratum 3 guarantees frequency accuracy based on a past locked value for the next 24 hours that will not exceed 0.37 ppm.

Like holdover, freerun is an unlocked mode. However, the output frequency is unrelated to locked history–instead, it is only guaranteed to be within a nominal value again related to the stratum level.

For example, freerun for a stratum 3 module guarantees an output frequency somewhere within 4.6 ppm of nominal. Both these modes are the 'ledges' to hang onto when there is no valid reference available. Returning from freerun or holdover to lock is also crucial, since returning too fast can result in a downstream transient.

Switching between the three modes may be done manually or automatically. Manual switching allows the designer to control the state of the module based on inputs either received from the module or derived externally. Output alarms from the module, such as loss-of-reference and loss of lock, are common alarms used for determining when to switch modes.

An additional feature is the automatic switching or autonomous operation that automatically controls the switching from one mode to the other. State indications allow the host board to monitor and react to what is going on internally.

Configurations

Power consumption and packaging are also important factors. Voltage requirements for these modules are either 5 or 3.3V. Most modules are now 3.3V, since 5V distribution is rare and must be generated specially with a dc/dc converter.

Timing modules typically come in non-standardized custom packages although many vendors are now supplying stratum 3 devices in an 18-pin 2 x 2 x 0.5-in. square package. Future packages based on a connector footprint are in demand because they are easier to upgrade or replace. Line card modules are usually much smaller. A common package is the 0.8 x 0.8x 0.35-in. SMT package.

Specialized ICs are available to handle the timing and synchronization functions. These task can appear simple when applying these ICs, but more often than not, the tasks are not that simple, and verification of the timing functions is more difficult on the host board, especially in the early stages of production creating delayed problem discoveries until final tests.