

THE CONNOR-WINFIELD CORPORATION



# System Synchronizing ICs with Analog PLL and Low Jitter Outputs





Global Timing Solutions for Over 60 Years



Connor-Winfield Products are Designed and Produced in the USA



# At Connor-Winfield we

take exceptional pride in providing solutions to your frequency control design requirements. Our ongoing goal is to always supply you with the right solution for your product.

With this ever-prevailing philosophy, we will work with your design team to assure complete compatibility with your final product design — even if that product does not currently exist. By participating at the front end of your design cycle, we will recommend the exact product you need...or co-develop to match your exact and precise design requirements.

This Timing Product Guide is intended to as an overview of the full line of Connor-Winfield timing products. Please visit our website for a more comprehensive look at our product offering.

www.conwin.com

Celebrating 60+ Years of Timing Excellence

## Integrated Timing Solutions -

## "System Synchronizing IC with Analog PLL and Low Jitter Outputs"

Since 1963, Connor-Winfield (CW) has been a leader serving the OEM oscillator and crystal marketplace. Since its inception, CW has continued to develop products and evolve time and frequency technology in concert with the evolution of communication systems. Total timing system design became the natural evolution of Connor-Winfield's experience and expertise. Incorporating proven crystal, VCXO, TCXO and OCXO and PLL technologies into system level designs, CW is able to control the fundamental requirements of communication system support. With its 55+ year history of precision frequency control and low noise signal generation, Connor Winfield is in a unique position to provide complete timing systems for network timing sync architecture, frequency regeneration and timing signal generation. Connor-Winfield's timing architecture began with subsystems and module offerings, and now culminating in highly flexible programmable integrated circuits with second and third generation designs offering ultra-low jitter, programmable frequency outputs. Our system level focus eliminates the need for dedicated timing expertise and the need to engineer and test individual filters, clocks and control functions; dramatically reducing design time and accelerating time to market. You get a system level solution, complete and ready to perform within the precise parameters of network timing requirements and your system communications/control specifications. All Connor-Winfield network timing products are designed to meet and exceed Telcordia/ITU standards including GR-1244 and GR-253, as well as G.812, G.813, G.8262 and G.8263, G.8272 PTP and IEEE1588 specifications.

Frequency components such as clocks and crystals are used in a variety of electronic equipment, not all of which require the precision and low noise characteristics demanded by communication system applications. Connor Winfield's timing components have been designed specifically to support the mission critical requirements of today's most sophisticated network and communication systems. Connor Winfield, through its long history of direct customer involvement, understands the nuanced behavior and characteristics of the products it designs and manufactures as they relate to system level performance. This experience is incorporated into the products and services offered to our customers.

#### **Reference Design**

After a discussion to understand the architecture of your network element, Connor-Winfield engineers can recommend a timing solution that exactly matches your requirements. The reference design will then include an ASIC and Connor-Winfield software, along with a functional block diagram and recommendations for external components. This allows the OEM to lay the design out on their board and manage all aspects of the material supply of the components.

All Connor-Winfield network timing products meet Telcordia/ITU standards including GR-1244, GR-253, G.812, G.813, as well as G.8282 and G.8263 specifications.

### **Timing Synchronization ICs:**

In distributed systems, time synchronization is a critical aspect of system operation. It ensures a common understanding of time order across the system, allowing processes to be coordinated accurately and reliably. Some systems use GPS signals to achieve time synchronization. The GPS satellites carry extremely accurate atomic clocks, and a GPS receiver can use the time signals from multiple satellites to synchronize its own clock to GPS time, which is closely aligned with UTC. The follow-ing ICs are designed to lock to 1PPS signals and generate synchronized, phase locked and frequency aligned outputs

The NS3D02 is a highly integrated time and frequency synchronizing IC designed to receive a 1PPS reference input and generate a 1PPS output and up to two single ended clock outputs phase locked and aligned to the rising edge of the 1PPS output pulse. This high precision phase and frequency synchronization solution integrates low phase noise frequency clock translation.

#### Features

- Phase locks to one incoming 1 PPS Reference input
- Generates two (2) single ended Low Jitter Clock Outputs derived from external VCXO
- Precision phase alignment of frequency outputs to 1 PPS phase locked output
- Internal phase error adjustment available for sawtooth error smoothing
- Flexible status indicators for Lock and LOS/ Holdover conditions.
- Flexible external 10MHz MCLK/Holdover options available.
- External VCXO supports up to 160 MHz clock output frequency range
- Programmable output dividers from external VCXO frequency
- Automatic compensation of external CC correctable OCXO module
- Programmable NPLL bandwidth settings for 1PPS disciplining
- I2C Interface for system communication and programming.
- 3.3VDC Supply Voltage
- -40°C to 105°C operating temperature range
- 5 x 5mm 40 pin QFN surface mount package

NS3D02



GPS/GNSS 1PPS Time to Clock Output Synchronizer

The NS2000-1PPS is a highly integrated time and frequency synchronizing ASIC. This design implementation is dedicated for use in applications which specifically require locking to an incoming 1PPS reference signal. This high precision phase and frequency synchronization solution also integrates low noise frequency generation and/or frequency translation. This product can be used to support a high-stability frequency reference for use in wireless systems, IEEE 1588v2, and applications employing a 1PPS frequency source for high precision, long term time and frequency generation.

#### Features

- Accepts 1 PPS Reference input
- Programmable phase alignment of outputs to 1 PPS reference input
- Internal NCO for SAW tooth error smoothing
- Locked, HO, & Free-run indication. Holdover options available to .001ppb resolution
- 1Hz to 800 MHz clock output frequency range
- Ten differential or up to 23 single ended Low Jitter Clock Outputs
- Programmable output transmitters (programmable as either 1 LVPECL, 1 LVDS or 2x LVCMOS output)
- Low jitter clock outputs (less than .3ps RMS (12kHz to 20MHz) with options for sub 100fs)
- Programmable bandwidth settings for multiple applications
- I2C Interface for system communication and interrogation.
- 3.3VDC Supply Voltage
- -40C to +85C operating temperature range
- 10 x10 mm 88 pin QFN surface mount package

The NS2D04-1PPS is a highly integrated time and frequency synchronizing ASIC. This design implementation is dedicated for use in applications which specifically require locking to an incoming 1PPS reference signal. This high precision phase and frequency synchronization solution also integrates low noise frequency generation and/or frequency translation. This product can be used to support a high-stability frequency reference for use in wireless systems, IEEE 1588v2, and applications employing a 1PPS frequency source for high precision, long term time and frequency generation.

#### Features

- Accepts 1 PPS Reference input
- Programmable phase alignment of outputs to 1 PPS reference input
- Internal NCO for SAW tooth error smoothing
- Locked, HO, & Free-run indication. Holdover options available to .001ppb resolution
- 1Hz to 800 MHz clock output frequency range
- Eight differential or up to 17 single ended Low Jitter Clock Outputs
- Programmable output transmitters (programmable as either 1 LVPECL, 1 LVDS or 2x LVCMOS output)
- Low jitter clock outputs (less than .3ps RMS (12kHz to 20MHz) with options for sub 100fs)
- Programmable bandwidth settings for multiple applications
- I2C Interface for system communication and interrogation.
- 3.3VDC Supply Voltage
- -40°C to 85°C operating temperature range

• 8 x 8 mm 68 pin QFN surface mount package



Complete Sync Timing System ASIC for Synchronous Ethernet / IEEE1588 Systems



GPS/GNSS 1PPS Time to Clock Output Synchronizer

## **Timing PLL ICs:**

PLL ICs-Frequency Translators/Clock Distribution Phase-Locked Loop (PLL) Integrated Circuits (ICs) are widely used in electronic systems for frequency translation and jitter cleaning. These applications span various fields, from telecommunications to consumer electronics.

The NF2004 is a highly integrated synchronizing ASIC for applications that require frequency translation, low noise jitter attenuation, multi output clock generation and clock synthesis. The design implementation is intended to be flexible offering multiple configurations that can be used to optimize low noise frequency generation and/or frequency translation.

#### Features

- Two Reference inputs (each can accept one LVCMOS reference signal/ clock)
- 1 Hz to 800 MHz clock output frequency range
- Eight differential or up to 17 single ended Low Jitter Clock Outputs
- Programmable output transmitters (programmable as either 1 LVPECL, 1 LVDS or 2x LVCMOS output)
- Low jitter clock outputs (less than .3ps RMS (12kHz to 20MHz) with optional configurations for sub 100fs performance
- I2C Interface for system communica tion and interrogation.
- 8 x8 mm 68 pin QFN surface mount package

#### **Typical Applications**

- Frequency Translation
- Clock smoothing
- Jitter Attenuation
- Clock Generation
- Wireless Base Stations
- GNSS Disciplined Oscillator

The NC2008 is a highly integrated multi output clock generator and signal translation device. This design implementation is extremely flexible in providing low noise frequency generation and/or signal level translation capability. The design architecture incorporates Connor-Winfield's second generation analog PLL technology to provide up to 17 output(s) at frequencies ranging from 1Hz to 800 MHz, depending upon the input reference option chosen. One or two external signal sources determine the output characteristics for phase noise and jitter performance for any combination of eight differential or 17 single ended clock outputs with output jitter performance options of sub 100fs RMS (12 kHz to 20MHz).

#### Features

- 1Hz to 800 MHz clock output frequency range
- Eight differential or up to 17 single ended Low Jitter Clock Outputs
- Programmable output transmitters (programmable as either 1 LVPECL, 1 LVDS or 2x LVCMOS output)
- 20 bit divider capability at output transmitters 1-8.
- . Low jitter clock outputs of less than .25ps RMS (12kHz to 20MHz) with options for sub 100fs.
- Signal translation from LVCMOS to LVPECL/LVDS or Vice versa
- External EEProm for loading or I2C Interface for system communication
- 3.3V supply
- 8x8 mm 68 pin QFN surface mount package
- -40C to +85C operating temperature range
- 10 x10 mm 88 pin QFN surface mount package

The NF1011 is a high performance frequency translator and jitter attenuator which is designed to meet requirements for multiple applications where low phase noise and ultra low jitter outputs are required including: frequency translation supporting wireless communication, 40G,100G and 400G Synchronous Ethernet, Sonet, OTN and IEEE 1588 network elements, clock translation with low phase noise, and other applications demanding sub-picosecond jitter performance.

#### Features

- Simple operation accepts one reference input and generates one output channel.
- Reference input accepts one single-ended 3.3V LVCMOS clock signal from 8 kHz up to 160 MHz.
- Generates one output channel based on the frequency of the external VCXO which drives one single-ended LVCMOS output with 6 bit divider circuit at Output transmitter.
- Accepts 3.3V LVCMOS VCXO input at frequencies from 10MHz to 160MHz.
- Internal multiple time programmable (MTP) memory bank.
- Programmable phase detector rate of PLL is minimum 8kHz to 500 KHz.
- Capable of <60fs jitter performance over 12kHz to 20MHz integration.
- Programmable Charge Pump current.
- Minimal external components required due to internal charge pump Caps.
- Supports I2C bus interface.
- Operating temperature range of -40°C to 85°C.
- 3.3V operation.
- 40-pin QFN package (5mm x 5mm)

NF1011



Frequency Translator and Jitter Attenuator



Synchronizing IC for Frequency Translation, Jitter Attenuation and Clock smoothing

NC2008



Multi Output Clock Generator IC

#### Legacy ICs — Synchronous Clock for SETS

The Legacy ICs, Phase-Locked Loop (PLL) Integrated Circuits (ICs) listed below were designed for full Network System Synchronization for applications supporting SONET and SDH and Synchronous Ethernet topologies. All ICs have freerun, holdover and reference switching capabilities. Control monitoring is done through an SPI bus..

The STC5230-I is RoHS 6/6 compliant and a single chip solution for the timing source in SDH, SONET, and Synchronous Ethernet network elements. The device is fully compliant with ITU-T G.813, G.8262, Telcordia GR1244, and GR253.

#### Features

- Suitable for SDH SETS, SONET Stratum 3, 4E, 4 and SMC, and Synchronous Ethernet
- Two timing generators, T0 and T4, for SETS
- Complies with ITU-T G.813 opt1/2, G.8262 EEC opt1/2, Telcordia GR1244 and GR253
- Supports Master/Slave for redundant application with the SyncLinkTM cross-couple data links
- Supports 4 different frequencies of external oscillator (programmable): 10MHz, 12.8MHz, 19.2MHz, 20MHz
- Accepts 12 individual clock reference inputs
- Supports automatically frequency detection or manually acceptable frequency. Each reference input is monitored for activity and quality
- · Supports manual and automatic reference selection
- 9 synchronized output clocks
- T0 and T4 have independent reference lists and priority tables for automatic reference selection

- Provides compensation for the phase delay of the master/slave cross couple links, in 0.1ns steps up to 409.5ns
- Provides measurement of the round-trip phase delay of the master slave cross-couple links.
- Phase align locking and hit-less reference switching
- Phase rebuild on re-lock and reference switches
- Programmable loop bandwidth (T0/T4) 0.1Hz to 103Hz
- Supports SPI bus interface
- Field upgrade capability
- IEEE 1149.1 JTAG boundary scan
- Available in TQFP100 package



The STC5420 is RoHS 6/6 compliant and a single chip clock synchronization solution for applications in SDH/SETS, SONET, and Synchronous Ethernet network elements. The device is fully compliant with ITU-T G.813 option 1 and 2, G.8262 EEC Opt1 and Opt2 and Telcordia GR1244 and GR253.z

#### Features

- Complies with ITU-T G.813 Opt1/Opt2, G.8262 EEC Opt1/Opt2, Telcordia GR1244 and GR253 (Stratum3/4E/ 4/SMC)
- Supports frequency auto detection or manually acceptable frequency for reference inputs. Each of them is monitored for activity and quality
- Two timing generators T0 and T4; T4 may lock to T0's synchronized output
- Supports Master/Slave and Multiple-Master redundan application (T0 timing generator only)
- Provides programmable compensation for phase delay between master and slave unit, in 0.1ns steps
- Accepts external oscillator at frequency of 10MHz, 12.8MHz, 19.2MHz,or 20MHz with programming
- Accepts 12 clock reference inputs
- Automatic/manual/hard-wired manual reference select
- Outputs 10 synchronized clock outputs, including 2 frame pulse clocks CLK8K and CLK2K

- 10 clock synthesizers generate frequencies
- Programmable phase skew in synthesizer level
- Phase-align or hit-less reference locking/switching
- Programmable loop bandwidth, from 0.1Hz to 100Hz
- · Supports bus interface: Intel, Motorola, Multiplex, SPI
- Single 3.3V operation
- IEEE 1149.1 JTAG boundary scan
- Available in TQFP100 package





The STC3800 is an integrated single chip solution for the Synchronous Timing Source in SONET/SDH network elements. The device generates four synchronous clocks, including BITS, and is fully compliant with Telcordia GR-1244-CORE, GR-253-CORE and ITU-T G.812/G.813.

#### Features

- Complies with Telcordia GR-1244-CORE, R-253-CORE, and ITU-T G.812/G.813
- Supports Master/Slave operation
- Four output signals: one selectable up to 155.52 MHz, one fixed at 8 kHz, one multi-frame sync fixed at 2 kHz, and 1.544 MHz or 2.048 MHz BITS output
- Supports Free Run, locked, and Hold Over modes
- Accepts 8 reference inputs and one cross reference each from 8 kHz to 77.76 MHz
- · Continuous input reference quality monitoring
- Input reference frequency are automatically detected
- Automatic or manual selection for active reference
- Supports hardwire pins to select active reference

- Output phase is adjustable in slave mode
- Frequency ramp control during reference switching
- Hit-less reference switching
- Better than 1 ppb Hold Over accuracy
- Configurable bandwidth filter for Stratum 3 or 3E
- Supports SPI and 8-bit parallel bus interface
- IEEE 1149.1 JTAG boundary scan
- Available in FBGA144 package



**STC3800** 

# Key Applications for Connor-Winfield's Time Synchronization products

#### 1. Telecommunications

GPS provides a time standard for telecom networks. Synchronization is crucial for network operations, including handoff between cell towers, time division multiple access (TDMA), and synchronization of data packets in networks.

#### 2. Power Grids

GPS time synchronization is used to coordinate the operation of power stations and substations. Precise timing helps in grid management, fault analysis, and load balancing.

#### 3. Financial Systems

Financial markets use GPS time stamps for transaction timing. This synchronization ensures a fair and orderly trading environment, which is particularly important for high-frequency trading (HFT) where milliseconds can make a significant difference.

## 4. Broadcasting

GPS timing is essential for synchronizing broadcast signals, particularly in networks that use Single Frequency Network (SFN) technology. Accurate timing ensures that the content broadcast from different transmitters remains in phase, avoiding signal overlap and interference.

#### 5. Satellite Communications

Precise timing is essential for satellite communication systems. GPS time synchronization is used to ensure proper timing of the signals transmitted and received by communication satellites.

#### 6. Data Centers

GPS is used to provide a precise time source for data centers, which is important for time-stamping data, synchronizing server operations, and managing data flows.

#### 7. Transportation Systems

GPS timing is used in various transportation systems, including air traffic control, where precise timing ensures the safety and efficiency of flight operations.

#### 8. Seismic Monitoring

In seismology, GPS timing is used to accurately timestamp seismic events. This is crucial for locating the epicenter of earthquakes and understanding seismic activity patterns.

#### 9. Military Operations

GPS timing is critical for various military applications, including coordinating operations, navigating, and targeting in precision-guided munitions.

### **10. Scientific Research**

Many scientific experiments, particularly in physics and astronomy, require precise timing for data collection and experiment synchronization. GPS provides a universally accessible and precise time standard.

#### 11. Network Time Servers

Network Time Protocol (NTP) servers often use GPS as a reference time source to distribute accurate time over computer networks.

#### 12. Surveying and Geolocation

Precise timing is crucial for determining the exact position in high-precision surveying and geolocation applications.

# TIMING PRODUCTS COMPARISON

TIMING IC's: Sync, Frequency Translation, Jitter Attenuation and Multi Output Clock Generation

# of Input erence Frequency puts PLL

cy Analog # of Chains Outputs

Total Output # of Frequenies

Output Fracti equenies Integ

Fractional/ Integrator 12kHz-20MHz

Footprint # of Pins

1PPS Time Synchronization with Jitter and Frequency Translation

Master clock, NPLL, NCO, hitless switching, phase align	NS3D02	(PDF)	2	1PPS	1	3	1PPS, 8k-156.25MHz	Integer	100fs, 250 fs	5x5mm QFN40
Master clock, NPLL, NCO, hitless switching, phase align	NS2D04-1PPS	(PDF)	3	1PPS 1Hz-125MHz	2	18	1PPS, 1Hz-800MHz	Integer	100fs, 250 fs	8x8mm QFN68
Master clock, NPLL, NCO, hitless switching, phase align	NS2000-1PPS	(PDF)	1	1PPS 1Hz-125MHz	2	23	1PPS, 1Hz-800MHz	Integer	100fs, 250 fs	10x10mm QFN88

PLL Frequency Translator	Model Number	Data Sheet PDFs	# of Reference Inputs	Input Frequency PLL	# of Analog Chains	Total # of Outputs	Output Frequenies	Fractional/ Integrator	Phase Jitter 12kHz-20M	Footprint # of Pins
Jitter attenuating , 1 input 8/16 outputs	NF2004	(PDF)	1	8KHz-125 MHz	2	17	1.5KHz - 800 MHz	Integer	100fs, 250 fs	8x8mm QFN68
Jitter attenuating , 1 input, 1 output	NF1011	(PDF)	1	8KHz-125 MHz	1	1	10 MHz - 160 MHz	Integer	100fs, 250 fs	5x5mm QFN40

Clock Generator/Signal Translator	Model Number	Data Sheet PDFs	# of Reference Inputs	Input Frequency PLL	# of Analog Chains	Total # of Outputs	Output Frequenies	Fractional/ Integrator	Phase Jitter 12kHz-20MH	Footprint # of Pins
Crystal or clock signal input, differential/ single ended	NC2008	(PDF)	2	10 MHz-160 MHz	2	17	1.5 KHz - 800 MHz	Integer	100fs, 250 fs	8x8mm QFN68

PLL Frequency Translator with Auto Compensation	Model Number	Data Sheet PDFs	# of Reference Inputs	Input Frequency PLL	# of Analog Chains	Total # of Outputs	Output Frequenies	Fractional/ Integrator	Phase Jitter 12kHz-20MHz	Footprint # of Pins
Compensates TSE 10MHz MCLK input, translates outputs	FT3C02	(PDF)	0	10 MHz	1	2	8KHz - 160 MHz	Integer	500 fs	5x5mm QFN40

DAC with Auto Compensation	Model Number	Data Sheet PDFs	# of Reference Inputs	Input Frequency PLL	# of Analog Chains	Total # of Outputs	Output Frequenies	Fractional/ Integrator	Phase Jitter 12kHz-20MHz	Footprint # of Pins
28 bit DAC with Auto-Compensation Capability	TDC210	(PDF)	1	5 MHz - 160 MHz	N/A	1	5 MHz - 160 MHz	N/A	N/A	5x5mm QFN40

Full System Synchronization	Model Number	Data Sheet PDFs	# of Reference Inputs	Input e Frequency PLL	# of Analog Chains	Total # of Outputs	Output Frequenies	Fractional/ Integrator	Phase Jitter 12kHz-20MHz	Footprint # of Pins
Programmable bandwidth .25mH to 10 Hz, 1PPS support	NS2000	(PDF)	3	1PPS, 1Hz-125MHz	2	23	1PPS, 1Hz-800MHz	Integer	100fs, 1 ps	10x10mm QFN88
Programmable bandwidth .25mH to 10 Hz, 1PPS support	NS2004	(PDF)	3	1PPS, 1Hz-125MHz	2	18	1PPS, 1Hz-800MHz	Integer	100fs, 1 ps	8x8mm QFN68

Legacy ICs, Full System Synchronization	Model Number	Data Sheet PDFs	# of Reference Inputs	Input Frequency PLL	# of Analog Chains	Total # of Outputs	Output Frequenies	Fractional/ Integrator	Phase Jitter 12kHz-20MHz	Footprint # of Pins
Full Stratum and Sync E compliance, 2 timing generators	STC5420	(PDF)	12	2KHz- 77.76MHz	0	8	2KHz -156.25MHz	Fractional	10 ps	TQFP 100
Master Slave, Autonomous Switching, Programmable	STC5230	(PDF)	12	2KHz- 77.76MHz	0	8	2KHz -156.25MHz	Fractional	10 ps	TQFP 100
Complete Stratum 3E timing system	STC3800	(PDF)	4	2KHz- 77.76MHz	0	4	2KHz -77.76MHz	Fractional	10 ps	BGA144

#### Support Oscillators for Connor-Winfield's Line of Timing ICs

#### V7223T VCXO Series

The Connor-Winfield V7223T Series models are 3.3V LVCMOS SMT 5.0x3.2mm voltage controlled crystal oscillators (VCXOs) with ultralow jitter. With LVCMOS outputs, the V7223T series is designed for PLL applications requiring high performance and low noise. These are particularly good for straight pass through applications and dividing directly from the VCXO frequency in the NS2000, NS2004 and NF2004. (also available in 3.2x2.5mm footprint).

Operating	Specifications	
Center Frequency (Fo)	50MHz – 156.25 MHz	Typical Phase Noise V7223T-100.0M
Operating Temperature Range	-40 - 85 °C	Phase Noise [dBc/Hz] Marker 1 [T1] Marker 2 [T1]   RF Atten 5 dB 1.0 Hz 1.00 Hz
Supply Voltage (Vdd)	3.3 Vdc	Top -60.08c/Hz 1 of 1 -71.7.08c/Hz -106.76.08c/Hz Spothobe Trivecovid Look Het: +31.2.36444t
Supply Current (Idd)	15 mA	
Absolute Pull Range:	±50ppm	
Integrated Phase Jitter (BW=12kHz to 20MHz)		
Fo=100MHz	60 fs RMS	
Fo=125MHz	60 fs RMS	
Typical Phase Noise for 100MHz		
SSB Phase Noise at 10Hz offset	70 dBc/Hz	ELL prove
SSB Phase Noise at 100Hz offset	105 dBc/Hz	
SSB Phase Noise at 1kHz offset	130 dBc/Hz	4.000FW 18HE
SSB Phase Noise at 10kHz offset	148 dBc/Hz	10 Hz 100 Hz 1 kHz 10 kHz 100 kHz 1 MHz 30 MHz Fingle av Offict
SSB Phase Noise at 100kHz offset	158 dBc/Hz	
SSB Phase Noise at 1MHz offset	163 dBc/Hz	
SSB Phase Noise at 10MHz offset	164 dBc/Hz	

#### **VBLD Series VCXO**

The Connor-Winfield VBLD Series models are 3.3V LVCMOS SMT 9x14mm voltage controlled crystal oscillators (VCXOs) using third overtone crystal technology to produce ultra-low jitter . With LVCMOS outputs, the VBLD series is designed for PLL applications requiring high performance and low noise. These are particularly good for straight pass through applications and dividing directly from the VCXO frequency in the NS2000, NS2004 and NF2004.

Operating	Specifications	
Center Frequency (Fo)	80MHz – 156.25 MHz	RFAtten 5 dB 10 Hz 100 Hz 1 kHz
Operating Temperature Range	-40 - 85 °C	- Top-ou dec/nz 1611 - /2/9 dec/nz0/7/6 dec/nz -155.43 dec/nz
Supply Voltage (Vdd)	3.3 Vdc	1 tdo. bdol. (+bd initial Holine
Supply Current (Idd) -	15 mA	3Q.000 M/VC VI65.33/2E0/Hz Ioc.
Absolute Pull Range:	±50ppm	
Integrated Phase Jitter (BW=12kHz to 20MHz)		
Fo=100MHz	70 fs RMS	
Fo=125MHz	70 fs RMS	
Typical Phase Noise for 100MHz		
SSB Phase Noise at 100Hz offset	110 dBc/Hz	
SSB Phase Noise at 1kHz offset	137 dBc/Hz	-160
SSB Phase Noise at 10kHz offset	158 dBc/Hz	
SSB Phase Noise at 100kHz offset	160 dBc/Hz	
SSB Phase Noise at 1MHz offset	160 dBc/Hz	Frequency Offset
SSB Phase Noise at 10MHz offset	160 dBc/Hz	

#### VL734T Programmable "Any Frequency" VCXO

The Connor-Winfield VL734T Series models are programmable 3.3V LVCMOS SMT 5x7mm voltage controlled crystal oscillators (VCXOs) using low noise PLL technology to produce ultra-low jitter clock outputs . With LVPECL or LVDS outputs, the VL734T series offers a frequency range from 10MHz to 2 GHZ with sub 150fs jitter performance. These are particularly good for straight pass through applications and dividing directly from the VCXO frequency in the NS2000, NS2004 and NF2004.

Operating	Specifications	Phase Noise [dBc/Hz] RF Atten 5 dB	Phase Noise Plot
Center Frequency (Fo)	10MHz – 2 GHz	Top -30 dBc/Hz	Fo=245.76 MHz
Operating Temperature Range	-40 - 85 °C		1d0.0d01865
Supply Voltage (Vdd)	3.3 Vdc		10.000 0002 +45523000002
Supply Current (Idd)	85 mA	-70	
Absolute Pull Range:	±100ppm		—
Integrated Phase Jitter (BW=12kHz to 20MHz)			
Fo=800MHz	140 fs RMS		er
Fo=245.76MHz	150 fs RMS	-130	EL1
Typical Phase Noise for 100MHz			EL, -
SSB Phase Noise at 1kHz offset	137 dBc/Hz		
SSB Phase Noise at 10kHz offset	158 dBc/Hz	LoopBW 11Hz	
SSB Phase Noise at 100kHz offset	160 dBc/Hz	10 Hz 100 Hz 1 kHz	10 kHz 100 kHz 1 MHz 30 MHz FreqtetoγOffset

## OCXO/TCXO Master Clock Options (for use with NS2000, NS2004, NF2004)

#### Precision OCXOs and TCXOs for Time and Frequency Sync Standards

V\*C223

VPLD

VBLD

IEEE-1588 TOP Precision Timing - Precision timing is more critical for the development of communication networks based on IEEE-1588 timing over packet (TOP) and 100/ 400 Gigabit Ethernet synchronization technologies. Connor Winfield developed its line of OCXOs and TCXOs to specifically support the emerging IEEE 1588 V2 standards as outlined by ITU-G.8262 Option 1 and Option 2 and ITU-G.8263, ITU-G.8272 and ITU-G.8273 as well as the traditional Sonet, SDN and OTN standards G.813 and GR-1244 Stratum 3 and Stratum 3E. Many frequency options are available from stock to support a variety of network synchronization designs. Follow the links below for stock availability.



150-200fs

50-60 fs

50-60 fs

Oscillator Class	A1	A2	C2	D	E
Superset Grouping			Stratum 3, SMC	Option 1 (SDH, Sync E)	Line Card
			& Option 2		
			(PDH, SONET, Sync E)		
Telecordia Clock	N/A	Stratum 3E	Stratum 3 for SONET	N/A	Stratum 4
	Type 1	Type III	G.813 Option 2	G.813 Option 1	
			G.8262 Option 2	G.8262 Option 1	
PLL Implied Bandwidth	3mHz	1mHz	0.1Hz	1Hz	14Hz
Free-run Accuracy (ppm)	N/A	±4.6	±4.6	±4.6	±32
Frequency Stability (pk-pk)	2	10	280	2000	N/A
at Variable Temperature (ppb)	_				,
Frequency Stability at	±0.2	±1	±40	±10	N/A
Constant Temperature (ppb)	-		-		•
Frequencies Available	10 MHz	10.0; 12.8;	10.0; 12.8; 19.2;	10.0; 12.8; 19.2; 20.0	Various
		20.0; 24.576 MHz	20.0; 24.576; 40.0 MHz	24.576; 40.0; 50.0 MHz	
Connor-Winfield Products					
Data Sheet Links	OX200SC-	OH100-600503CF	M602	M622	CWX
	10M	OH300-600503CF	T6-2	T622	Series
				DOC102F	

Master Clock Models Supporting CW Timing ICs								
OCXO Model #	Thermal Stability	ADEV	Temp Range	Footprint				
OH100-10M,20M, 24.576M	OH100-10M,20M, 24.576M 10ppb pk-pk, 5ppb available		Commercial/IT	25x25mm				
OH300-10M,20M, 24.576M	OH300-10M,20M, 24.576M 10ppb pk-pk, 5ppb available		Commercial/IT	25x36mm				
OH300-10M,20M, 24.576M	1300-10M,20M, 24.576M 10ppb pk-pk, 5ppb available		Commercial/IT	22x25mm				
OX200SC 10M 3ppb pk-pk		1.x10-11	Commercial	25x36mm				
OH4-24.576M, 20M, 19.2M 20ppb pk-pk		3x10-11	Commercial/IT	14x20mm				
DOCSC-24.576M/20M/19.2M 20ppb pk-pk		3x10-11	Commercial/IT	9x14mm				
TCXO Model # Thermal Stability		ADEV	Temp Range	Footprint				
T100	+/- 100 ppb	1x10-10	Commercial	5x7mm				
T200	+/- 200 ppb	1x10-10	Industrial	5x7mm				
TL602 +/- 140 ppb		1x10-10	Industrial	5x7mm				
T602	T602 +/- 280 ppb		Industrial	5x7mm				
T622 +/- 1ppm		1x10-10	Industrial	5x7mm				
DOT +/- 50ppb		1x10-10	Commercial	9x14mm				
VCXO Model #	Frequency Range	Output Logic	Footprint	Jitter Level				
V9223	2-50MHz	LVCMOS	3225	200 fs				
2M-50Mhz		LVCMOS	5032	200 fs				
VKB series	2M-80M	LVCMOS	7050	200 fs				
V7223T	50M to 156.25M	LVCMOS	5032	60-80 fs				
VB762	100-250M	LVPECL	7050	85 fs				

## **CLOCKS Supporting CW Timing ICs**

LVCMOS, LVPECL, LVDS

LVPECL

LVCMOS

9x14mm

9x14mm

10M-2 GHZ

400-700MHz

80-204.8M

	Clock Model Series	Frequency Range	Output Logic	Supply Voltage	Footprint
	XF Series	1-50M	LVCMOS	1.8V	2016
Yaz	XE Series	1-50M	LVCMOS	3.3V	2520
188 3 1213	XD Series	1-50M	LVCMOS	3.3Vdc	3225
	XC Series	1-50M	LVCMOS	3.3Vdc	5032
	X series	10M- 160M	LVCMOS	3.3Vdc	7050
	FPC series	1M-2GHz	LVPECL/LVDS/CMOS	Programmable (factory)	7050
-	XPC series	1M- 2GHZ	LVPECL/LVDS/CMOS	Programmable On board I2C	7050

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THE CONNOR-WINFIELD CORPORATION



Headquarters at 2111 Comprehensive Dr. Aurora, IL



Manufacturing Facility at 2359 Diehl Rd, Aurora, IL

## **Our Partnership Philosophy**

Connor-Winfield talks about partnerships, but how do we follow through?

From design to delivery, we are committed to providing the right product when you need it to get your product to market. But the process is circular. We also track emerging developments in our customers' markets to ensure that we have the tools and data required to support your next product development effort



Check on-line for the most up to date RoHS

#### **The Connor-Winfield Corporation**

2111 Comprehensive Drive Aurora, Illinois 60505 Phone: 630-851-4722 sales@conwin.com



For specific product data, performance specifications, dimensions and ordering information, please refer to our website at www.conwin.com

ISO 9001:2015 Certification Connor-Winfield has been ISO 9001 certified since 1995, and is currently certified under ISO's newest



ISO 9001:2000 standard which ensures superior quality and repeatability in the manufacturing process. We believe that quality

begins well before our product is ever assembled. By maintaining our ISO 9001:2015 Quality System certification, continuous improvement to our processes is a commitment we make to constantly go beyond the expectations of our customers. For us, quality is not just a technique or system. It is an all encompassing and uncompromising philosophy to produce products that not only precisely meet our customers' quality requirements, but also surpass them in every way.